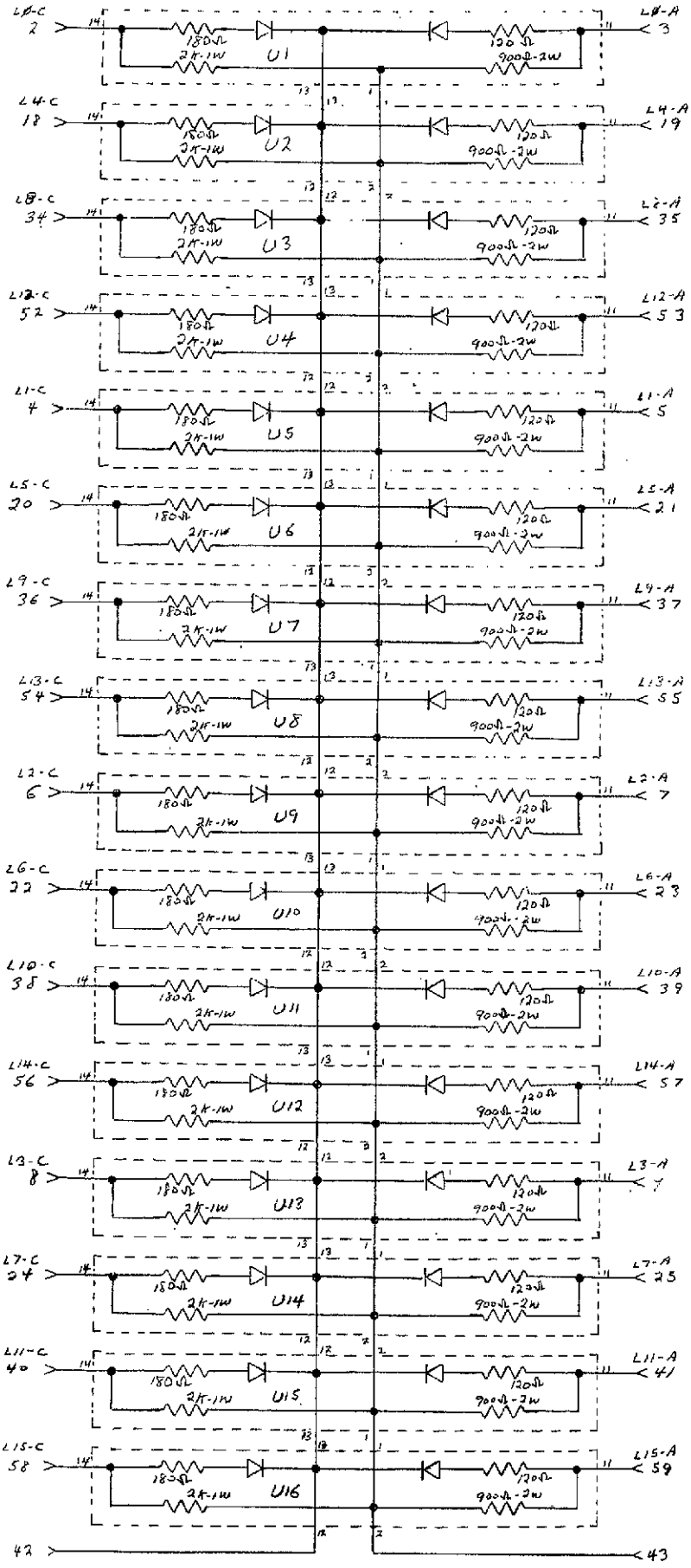


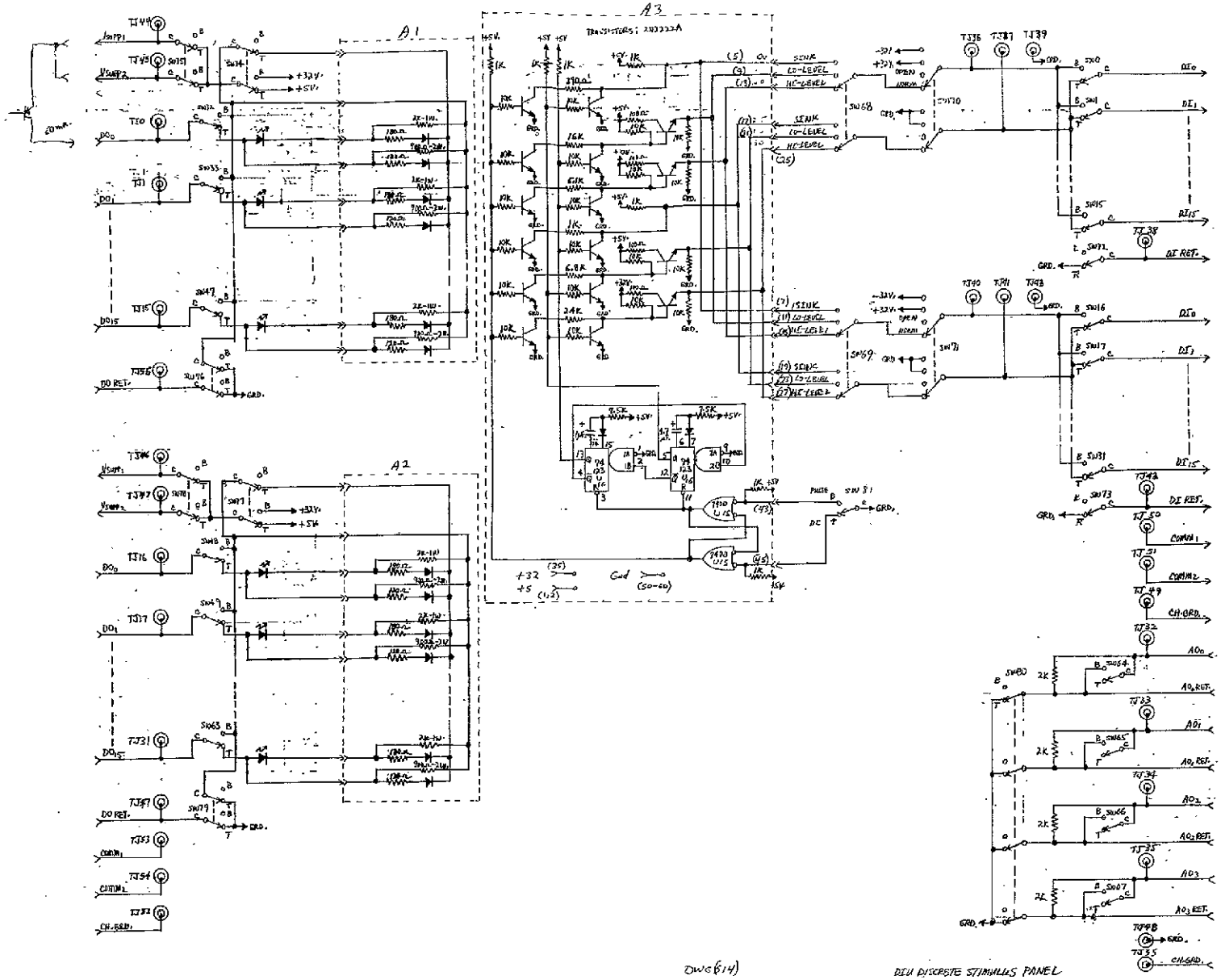
ALL SLOTS WIRED AS 16 PIN

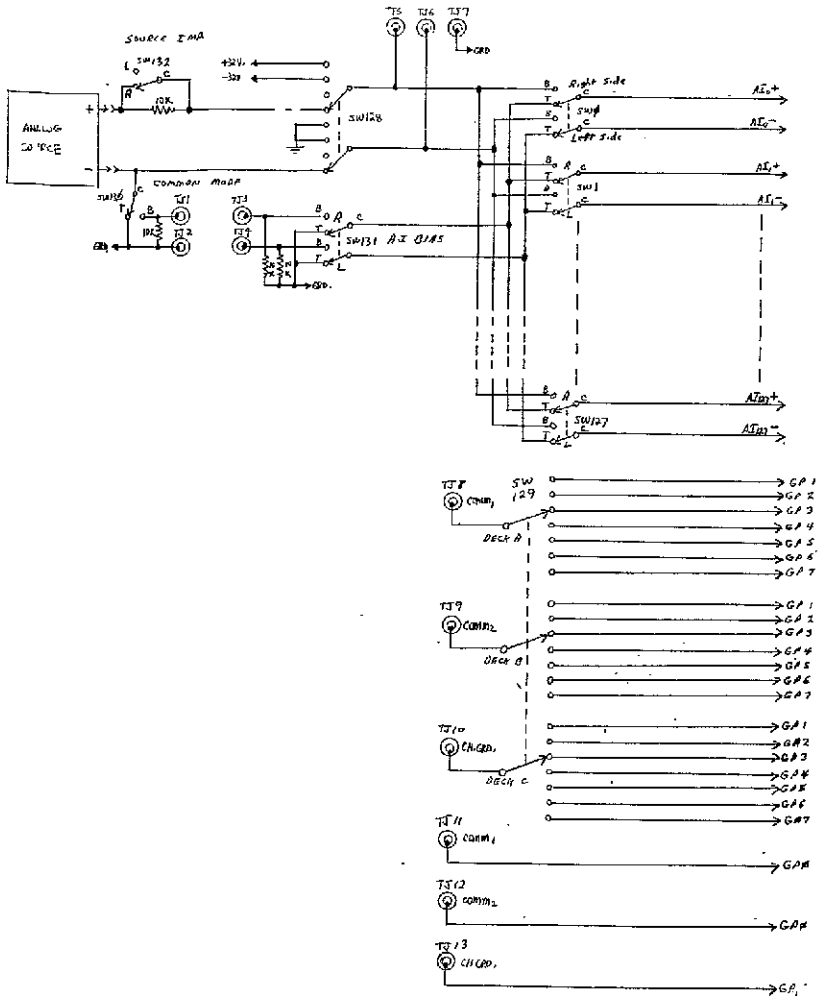
DIU T/S DI/DO/AO STIMULUS PANEL A1/A2

3339552

Diodes - 1N4454

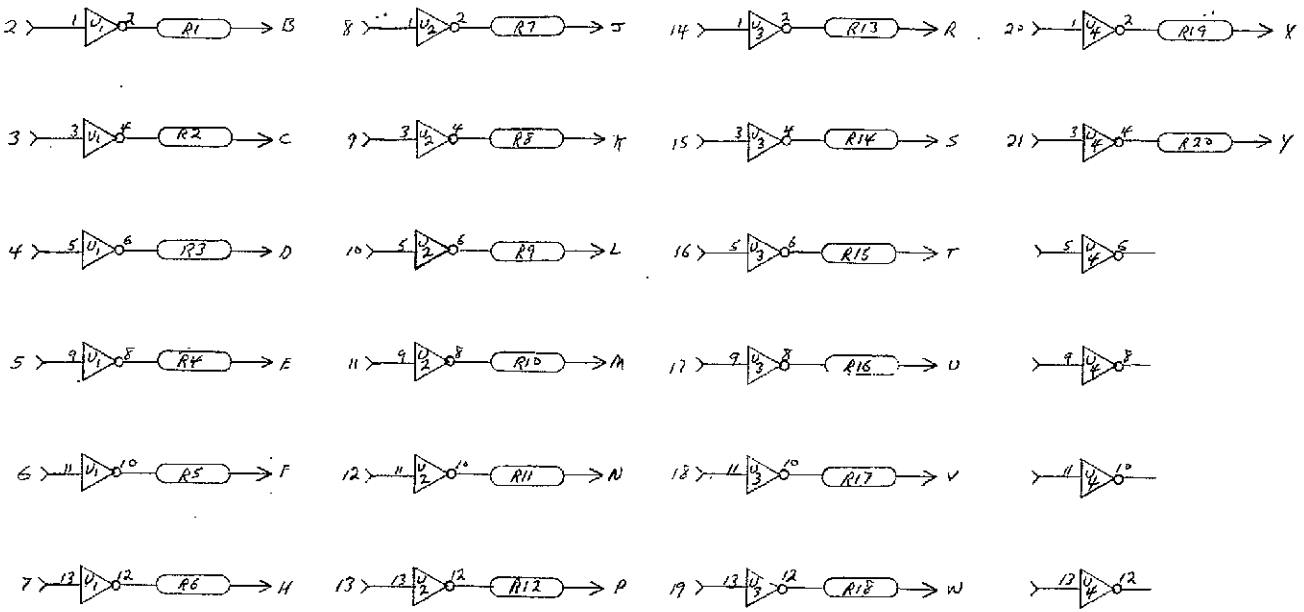
DWG 15

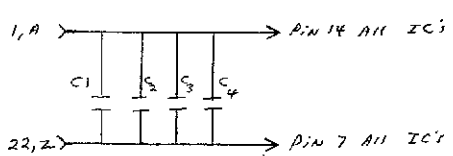

A1
A2
A3
TRANSISTORS; 2N3323A
DWG 614)
DIU DISCRETE STIMULUS PANEL
3339550



DIU ANALOG STIMULUS PANEL
3339 58-

Dwg(6-13)

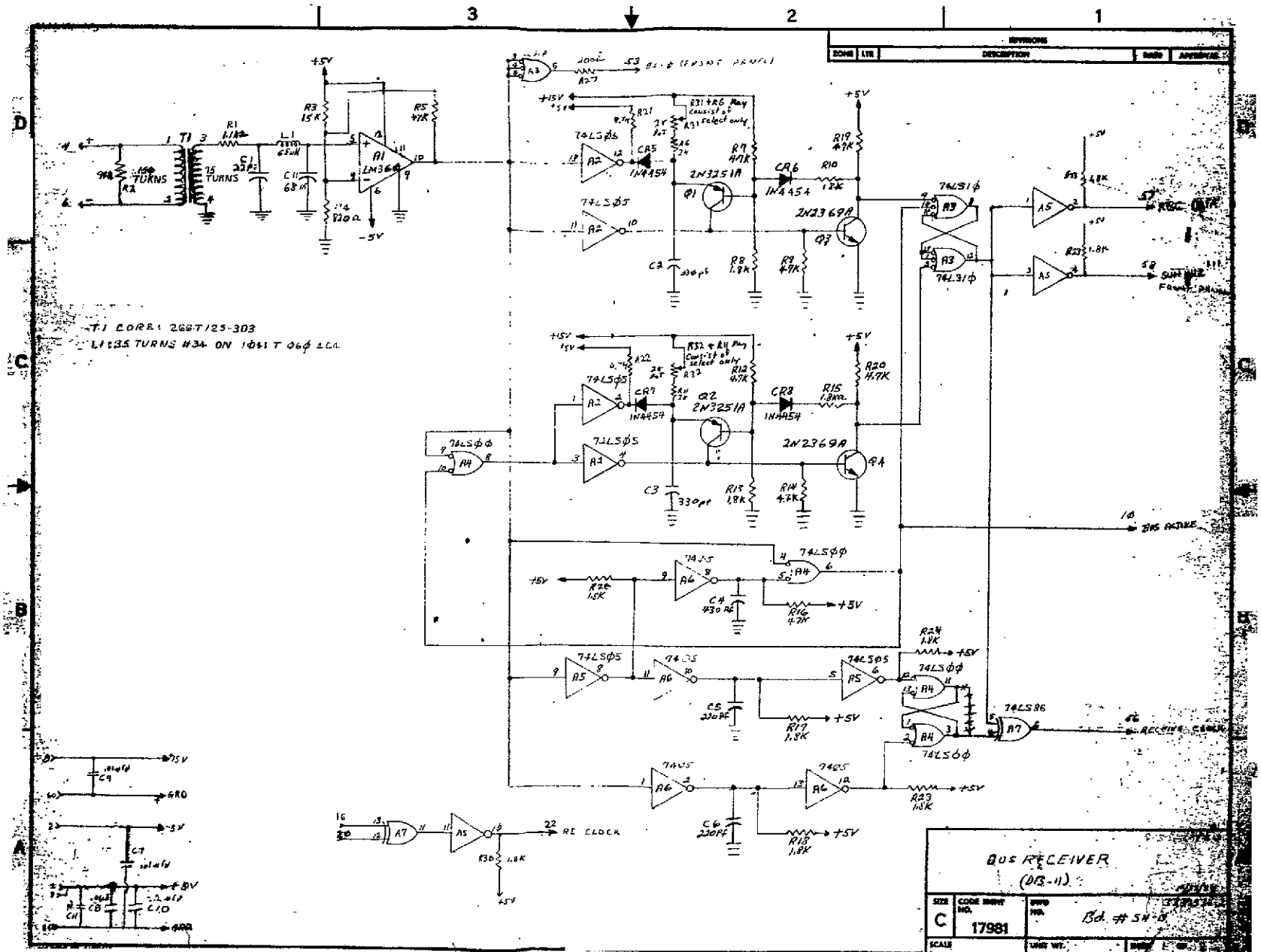




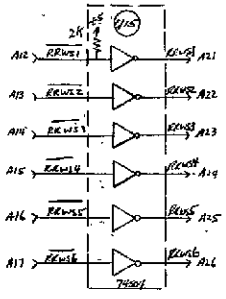
Parts		QTY.
U1-U4	SN7405N	4
R1-R20	RL07C0381J	20
C1	CS13BE156H	1
C2-C4	0.1/1002-103K	3

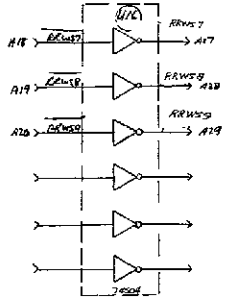
DIU TEST SET - TCU
LAMP DRIVERS
IBS1 - IBS5
3339532

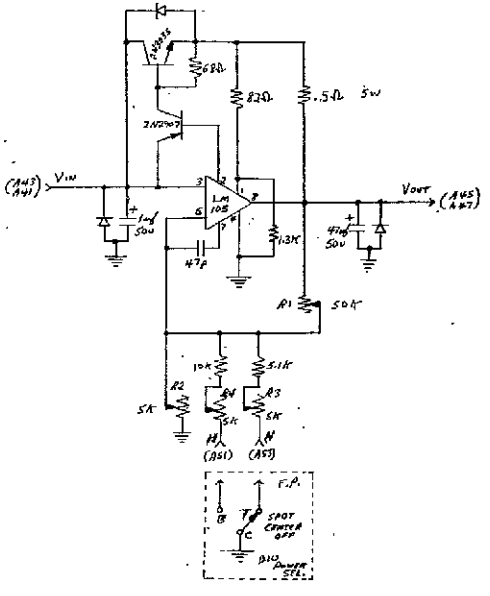
DWG-B12

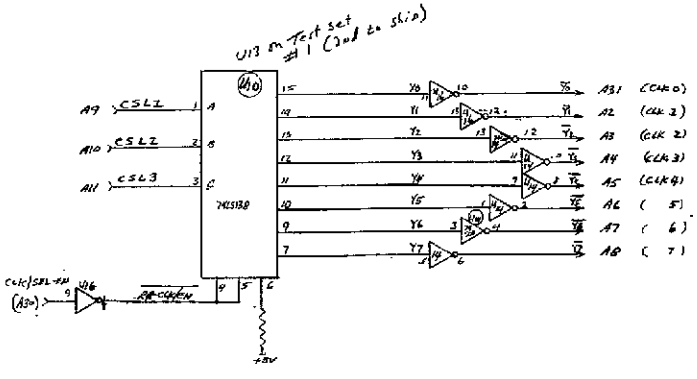

3
2
1
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
T1 CORE: 266T125-3D3
L1: 35 TURNS #34 ON 10Ω 1 T 06Φ ECO
T1
L1
C1
C11
A1
LM360
R1
R2
R3
R4
R5
Q1
Q2
Q3
Q4
CR5
CR6
CR7
CR8
C3
C4
C5
C6
R7
R8
R9
R10
R12
R13
R14
R15
R16
R17
R18
R19
R20
R23
R24
R26
R27
R30
R31
R32
74LSΦ5
74LSΦΦ
74LS86
74Φ5
74Φ35
2N3251A
2N2369A
1N4454
+5V
+15V
-5V
GND
RE CLOCK
BUS RECEIVER
(DB-11)
SIZE C
CODE IDENT NO. 17981
DWG NO. Bd. # SN-8
SCALE
WEIGHT
SHEET

PART NO.	IC #'S	TEST CONDITION	Vcc	GND
74S04	U13-U15,U16	5	14	7
74LS138	U9	1	16	8

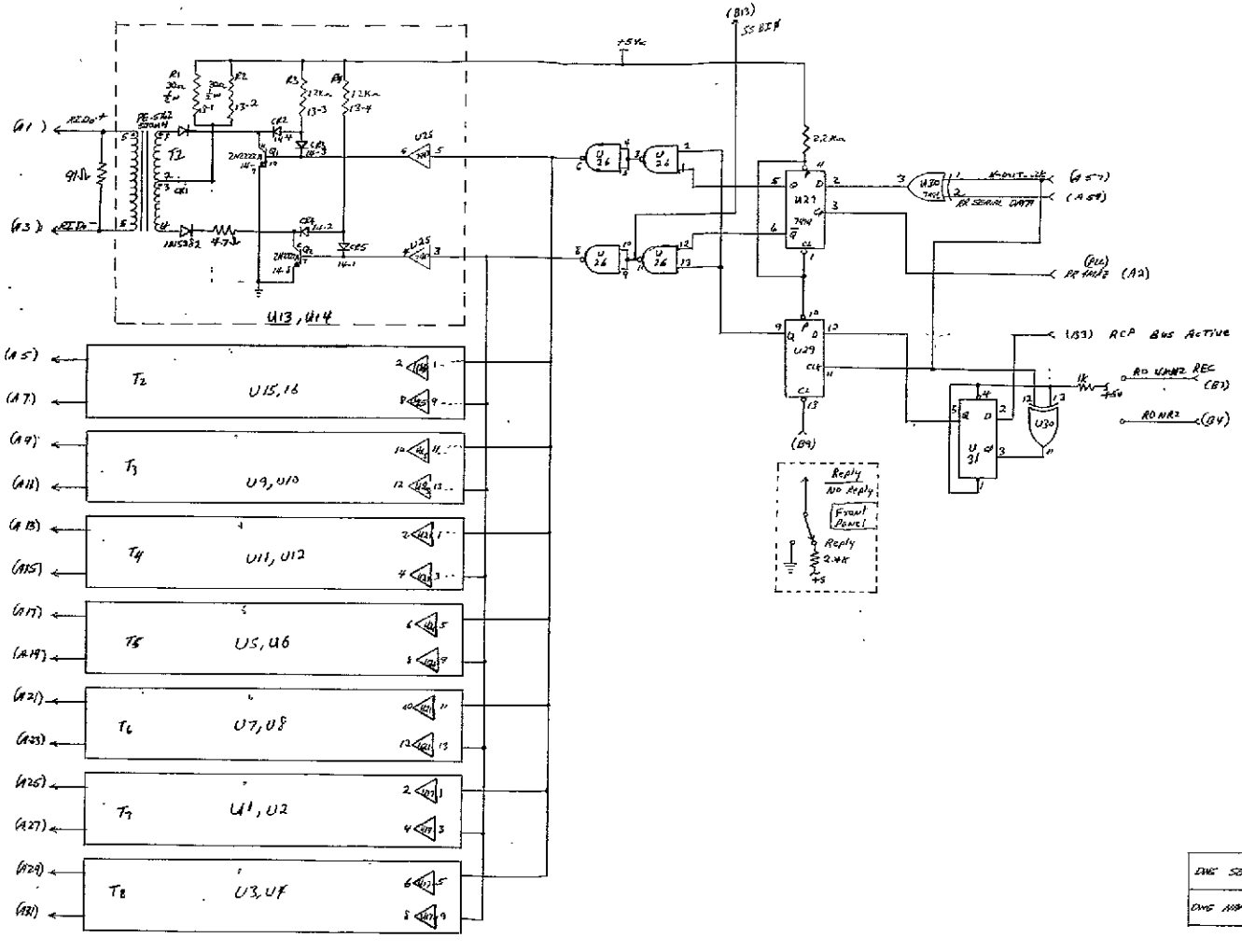








(1) 10-23-74
(2)
(3)
(4)
(5)

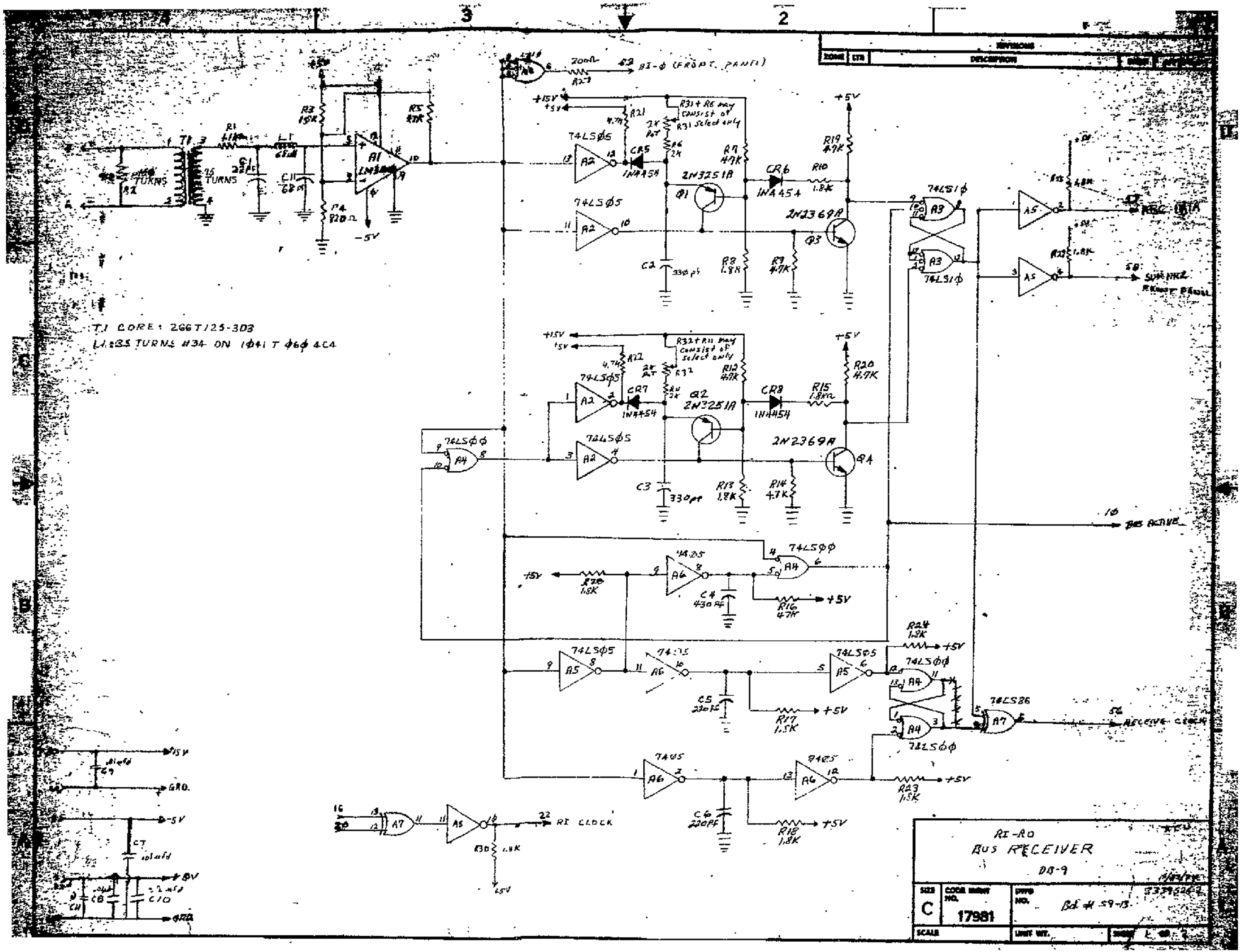


DWG SIZE	CDU TEST SET - TCU CARD C
DWG NAME	RE TRANSMIT

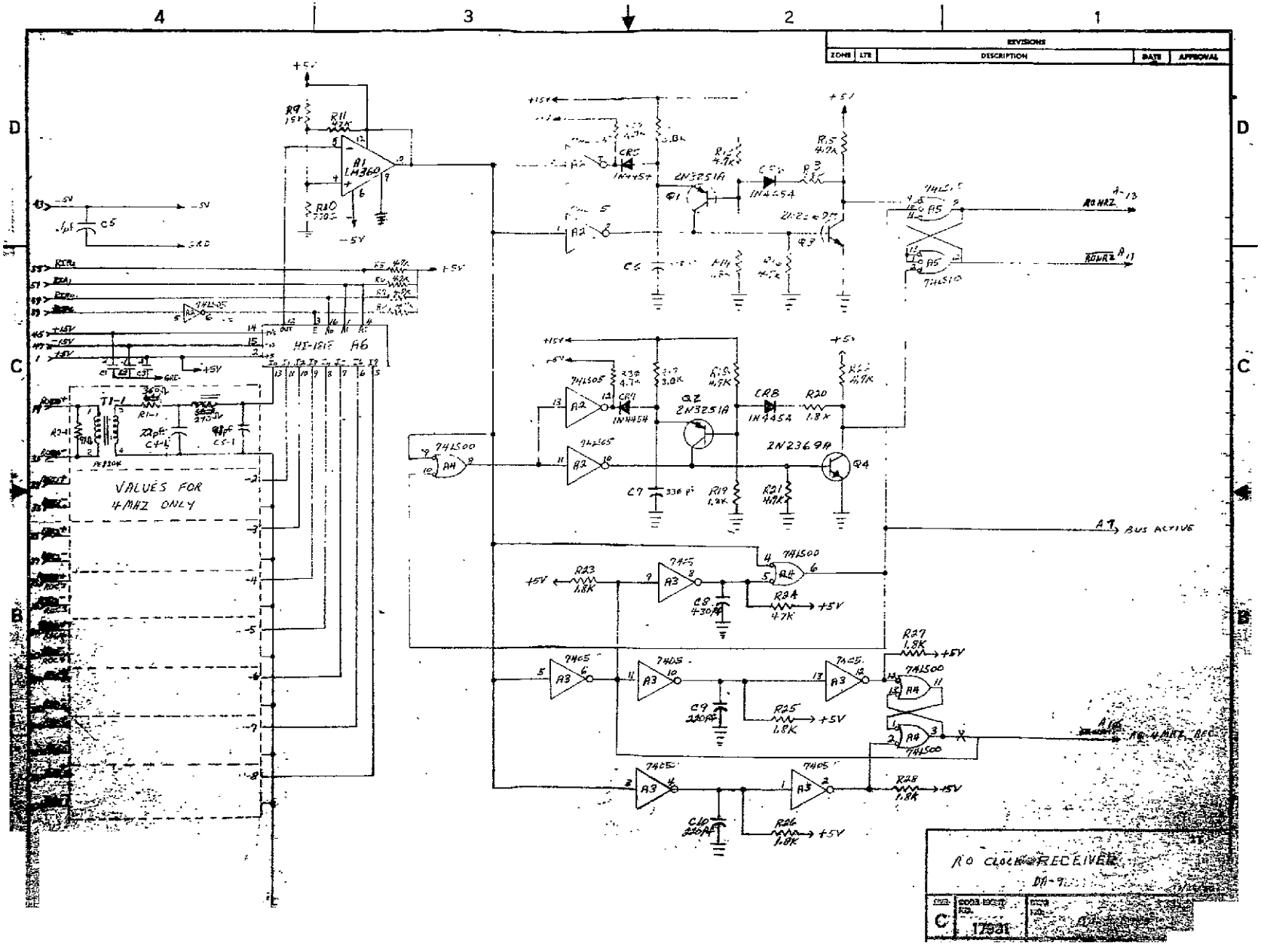
3339528

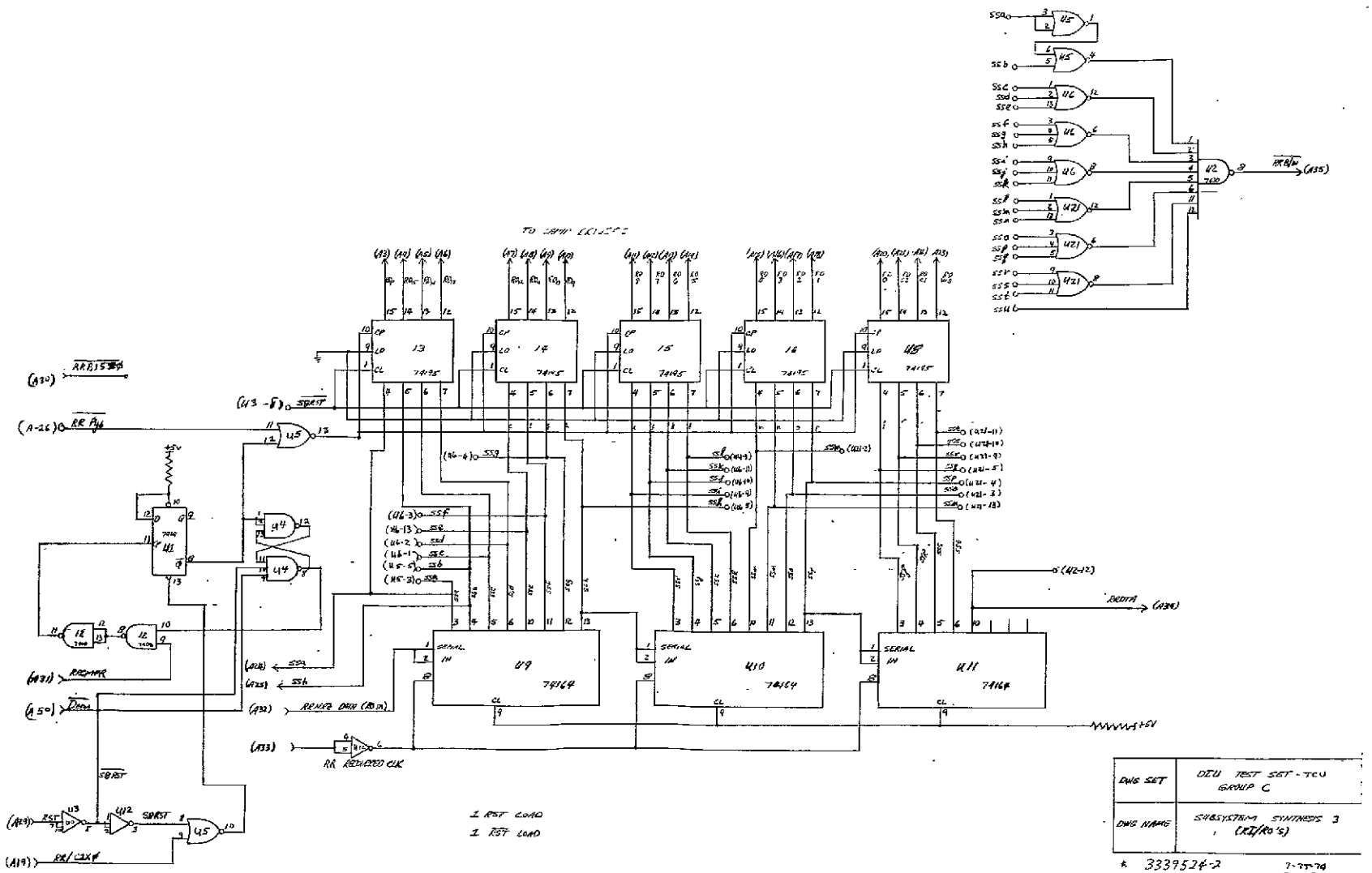
SIDE

BOARD POSITION 1 SLOT 5/10



3
2
REVISIONS
ZONE
LTR
DESCRIPTION
BI-Φ (FRONT PANEL)
R27
T1
TURNS
R1
L1
C1
C11
R3
R4
R5
A1
-5V
T1 CORE: 266T125-3D3
L1: 35 TURNS #34 ON 1Φ41 T Φ6Φ 4C4
+15V
+5V
R21
4.7K
R31 + R6 may consist of R31 select only
74LSΦ5
A2
CR5
1N4454
2N3251A
Q1
R7
47K
CR6
1N4454
R10
1.8K
+5V
R19
2N2369A
Q3
C2
R8
1.8K
R9
4.7K
74LS1Φ
A3
A5
REC DATA
SUM NRZ
R32 + R11 may consist of select only
R12
R22
CR7
CR8
R15
R20
4.7K
2N3251A
2N2369A
Q2
Q4
74LSΦΦ
A4
C3
330pf
R13
1.8K
R14
4.7K
BUS ACTIVE
A6
R28
1.8K
C4
R16
47K
R24
1.8K
74LS86
A7
RECEIVE CLOCK
C5
R17
1.5K
C6
220PF
R18
1.8K
R23
1.5K
RI CLOCK
R30
1.8K
+5V
-5V
GRD.
C9
C7
C8
C10
RI-RO
BUS RECEIVER
DB-9
SIZE
C
CODE IDENT NO.
17981
DWG NO.
Bd. # 59-13
SCALE
UNIT WT.
SHEET

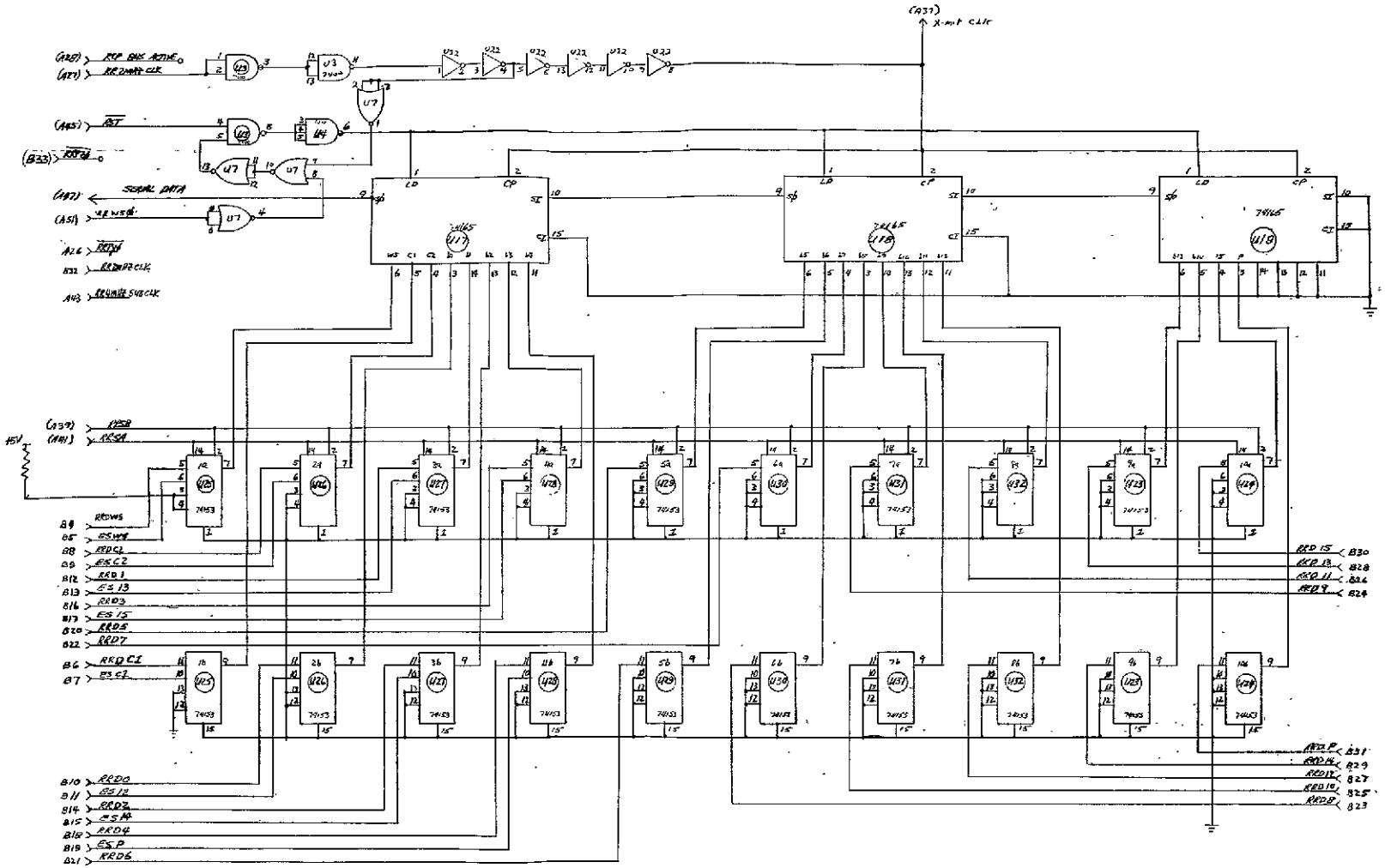

4
3
2
1
D
C
B
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVAL
+5V
-5V
GND
R9
15K
R11
A1
LM360
R10
750Ω
.1μF
C5
HI-1215 A6
VALUES FOR
4MHZ ONLY
T1-1
R1-1
R1-2
22pF
C4-1
47pF
C5-1
CR5
IN4454
2N3251A
Q1
Q2
Q3
R13
4.7K
R15
4.7K
C6
R14
4.7K
R16
4.7K
74LS05
A2
74LS00
A5
74LS10
A-13
A0 MHZ
A0 MHZ
A-13
CR6
IN4454
R20
1.8K
2N2369A
Q4
C7
330 pF
R19
1.8K
R21
47K
A7
BUS ACTIVE
74LS00
A4
74LS05
A3
R23
1.8K
C8
430pF
R24
47K
R27
1.8K
C9
220pF
R25
1.8K
R28
1.8K
C10
220pF
R26
1.8K
A10
TO 4 MHZ REC
A0 CLOCK RECEIVER
DA-9
C
17931



DWG SET	DEU TEST SET - TCU GROUP C
DWG NAME	SUBSYSTEM SYNTHESIS 3 (RX/RO'S)

* 3339524-2

7-27-79
8-16-79
9-14-79
9-26-79



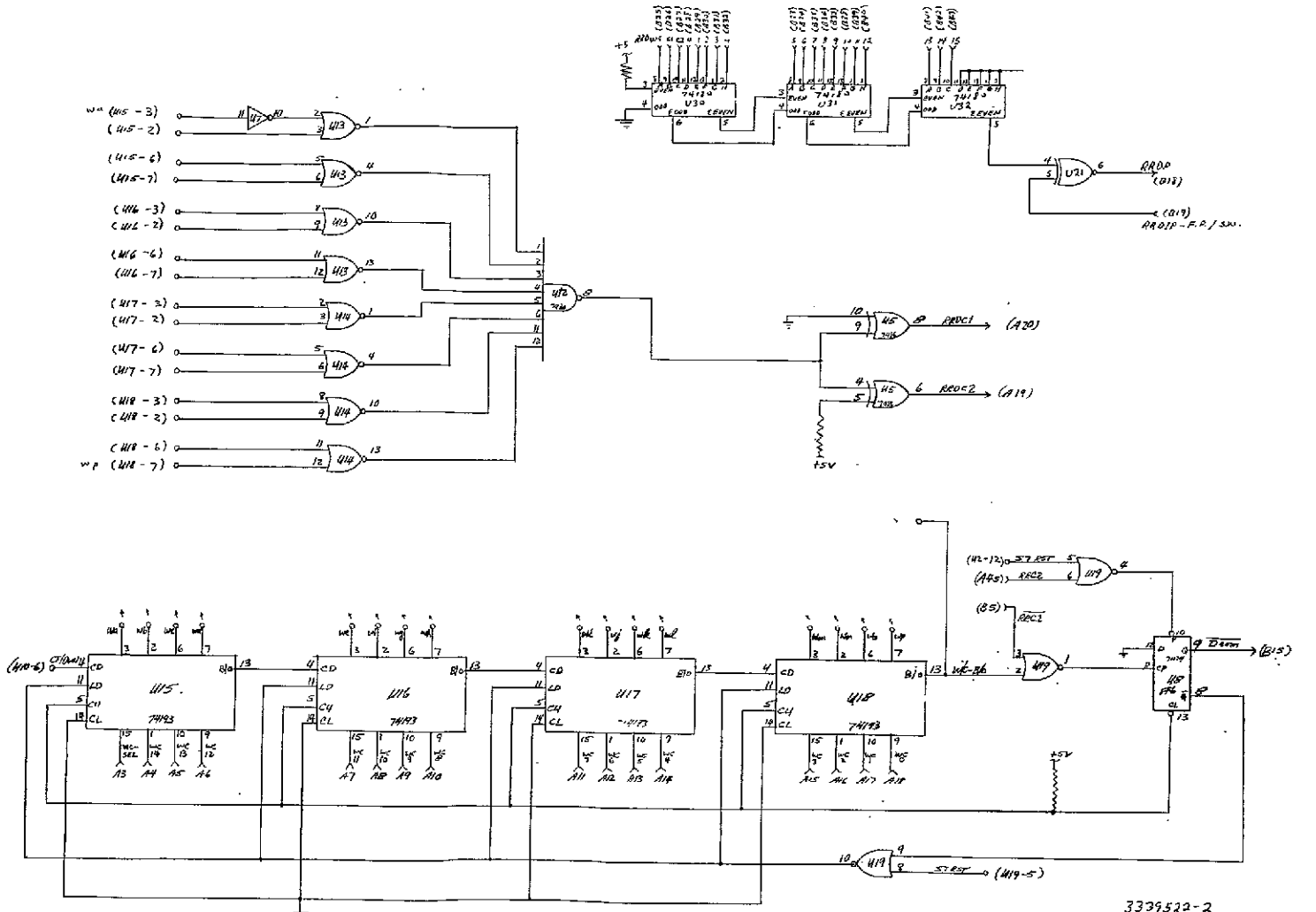
DWG. SET	DIU TEST SET - TCU GROUP C
DWG. NAME	SUBSYSTEM SYNTHESIS 3 (RT/ROS)

3339524-1

SP SHEET 'C'

CARD POSITION : SLOT SEP C

7-25-74
8-6-74
8-19-74
9-26-74

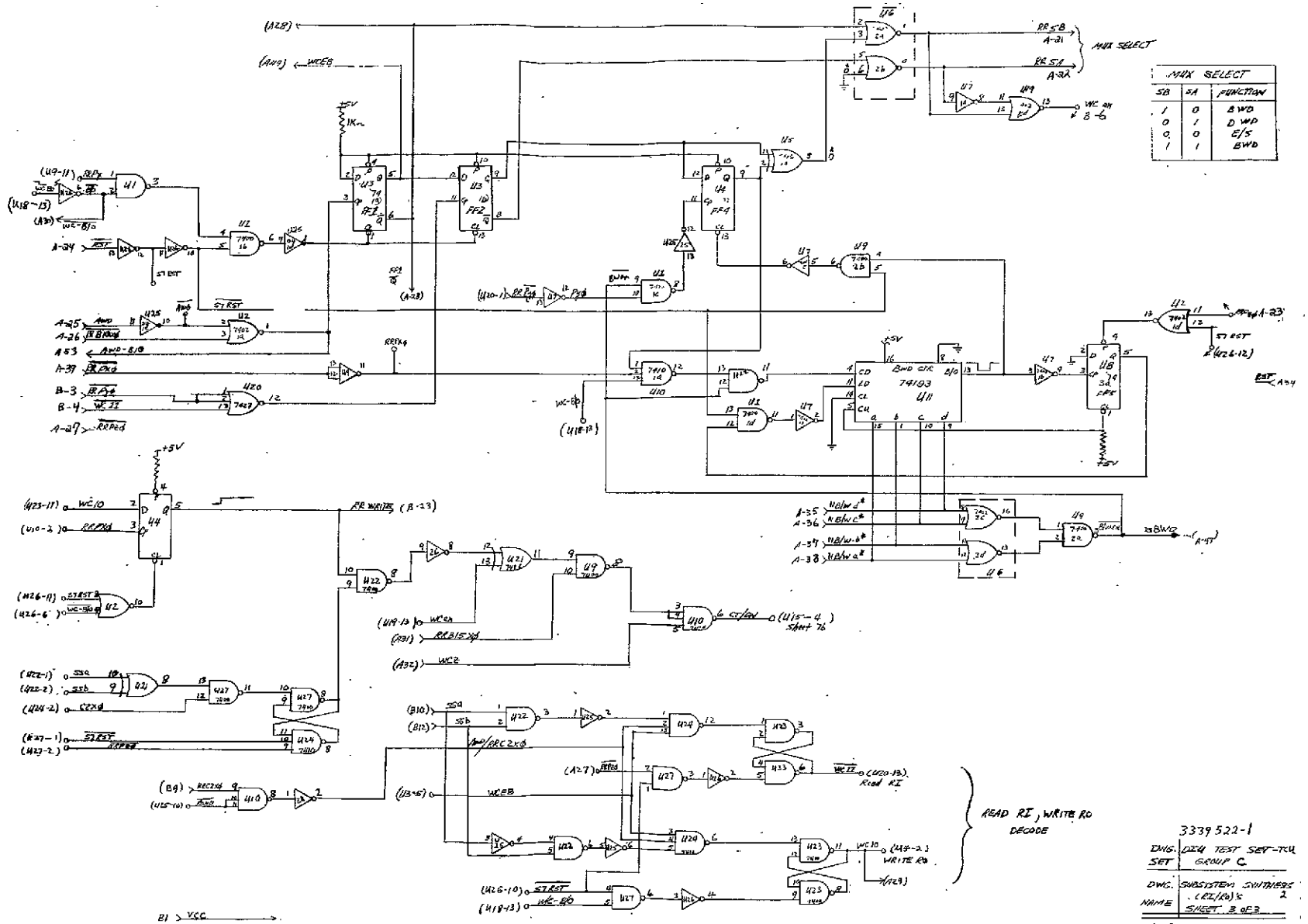


CARD POSITION : SLOT (S7)b

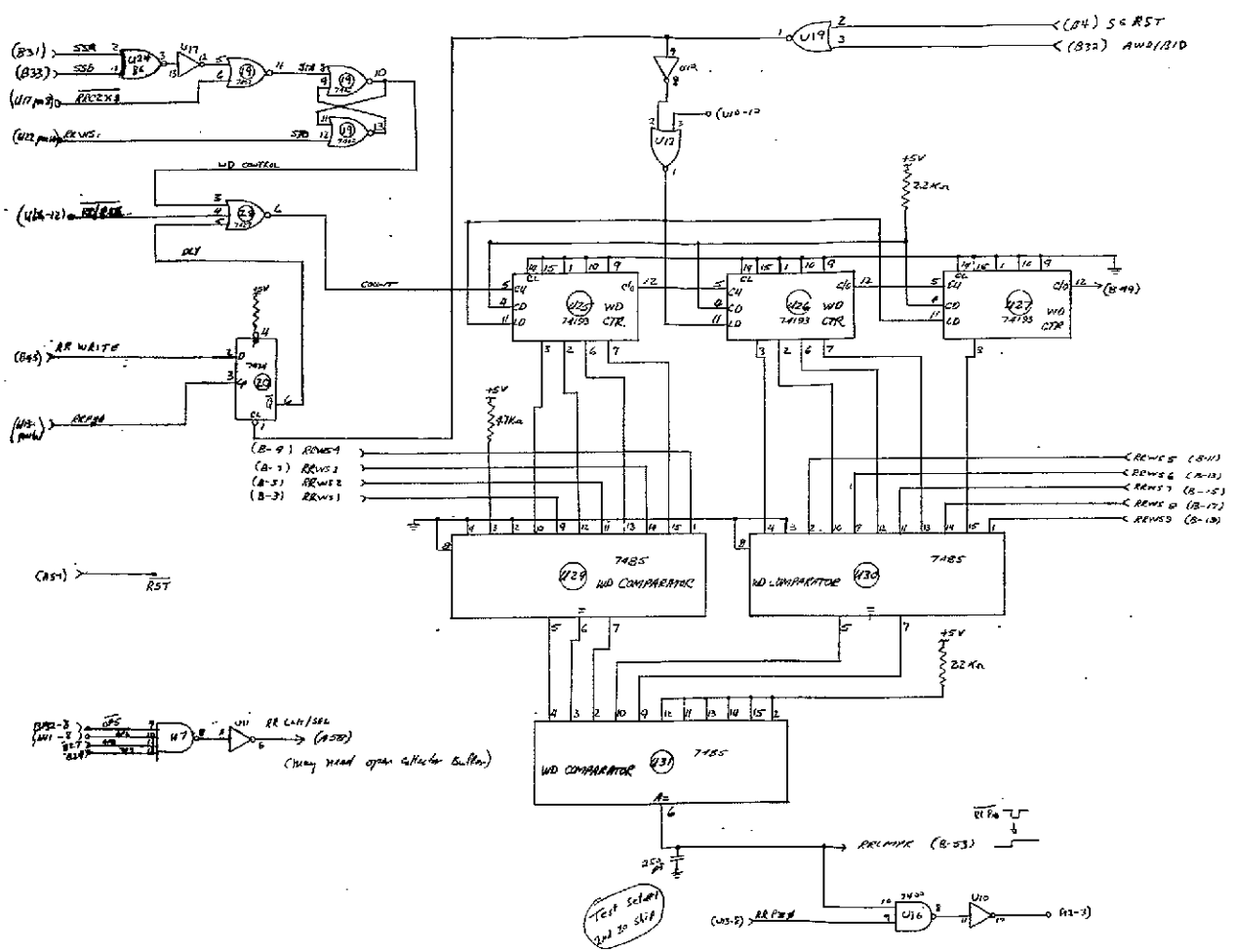
(S7-6)

	3339522-2
DWG. SET	IBM TEST SET - TCU GROUP C
DWG NAME	SUBSYSTEM SYNTHESIS 2 (RZ/RO 'S)

5-12-74
12-27-74


MUX SELECT
SB SA FUNCTION
1 0 BWD
0 1 D WD
0 0 E/S
1 1 BWD
READ RI, WRITE RO DECODE
3339522-1
DWG. SET: DC4 TEST SET-TCU GROUP C
DWG. NAME: SUBSYSTEM SYNTHESIS 2 (RI/RO)'S SHEET 3 OF 3
1 TRANSMIT SYNTHESIS
2 BLANK WORD CTR
3 LAST WORD DECODE
4 WORD COUNTER
CARD POSITION: SLOT 7
(57)a
(57-a)

Pin outs on Sheet 1A



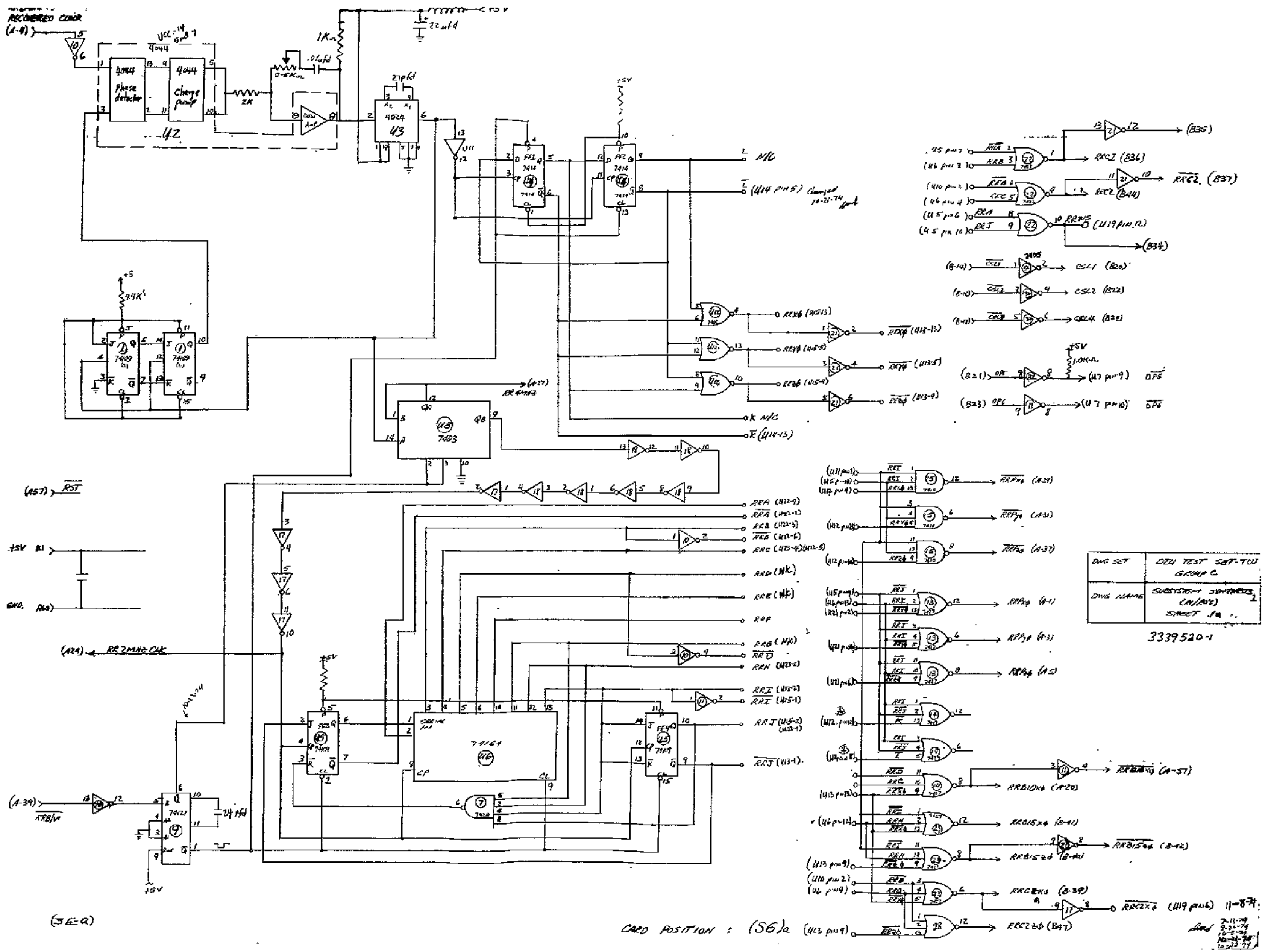
DWG SET	DIU TEST SET-TEU GROUP C
DWG NAME	SUBSYSTEM SYNTHESIS 1 RE NO 5 SHEET 1B

3339500-2

(56-6)

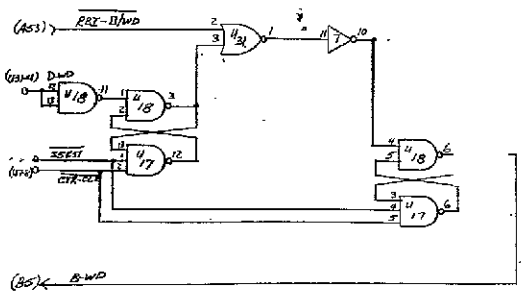
CARD POSITION 1 SLOT 6b (56)

7-13-79
9-24-79
10-2-79

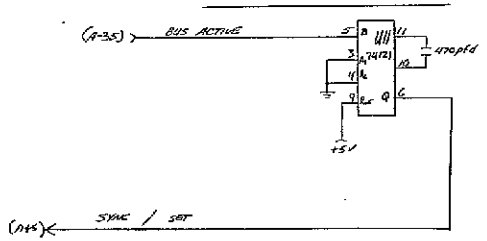


RECOVERED COLOR
4044
Phase detector
Charge pump
4024
7493
74164
7474
74121
RR 2MHz CLK
CARD POSITION : (S6)a
(SE-a)
3339520-1

BLANK WORD DISPLAY LOGIC



SYNC WORD COUNTER CONTROL

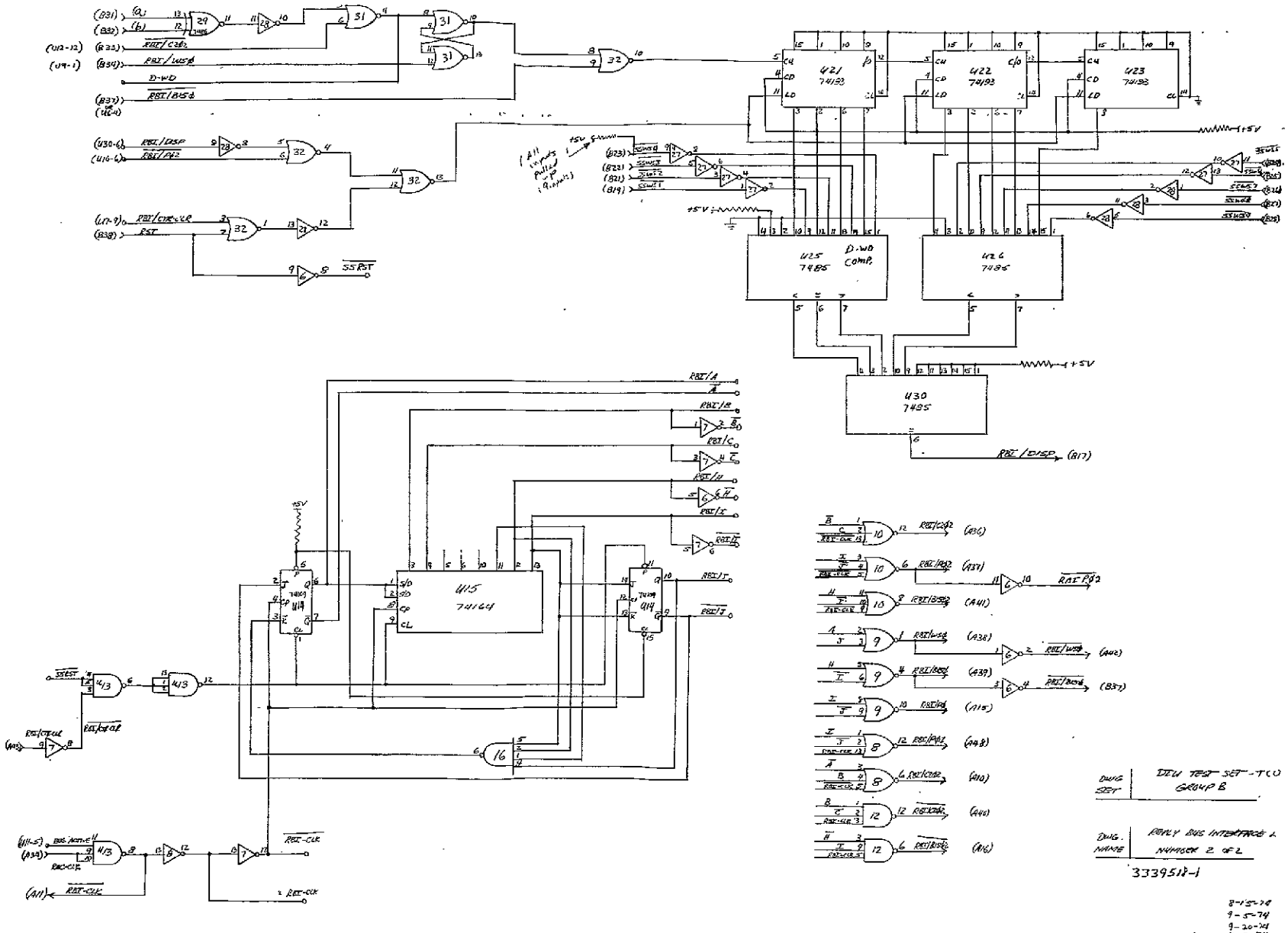


DWG SET	DEU TEST SET-TCU GROUP B
DWG NAME	REPLY BUS INTERFACE NUMBER 2 OF 2

3339518-2

1-31-75

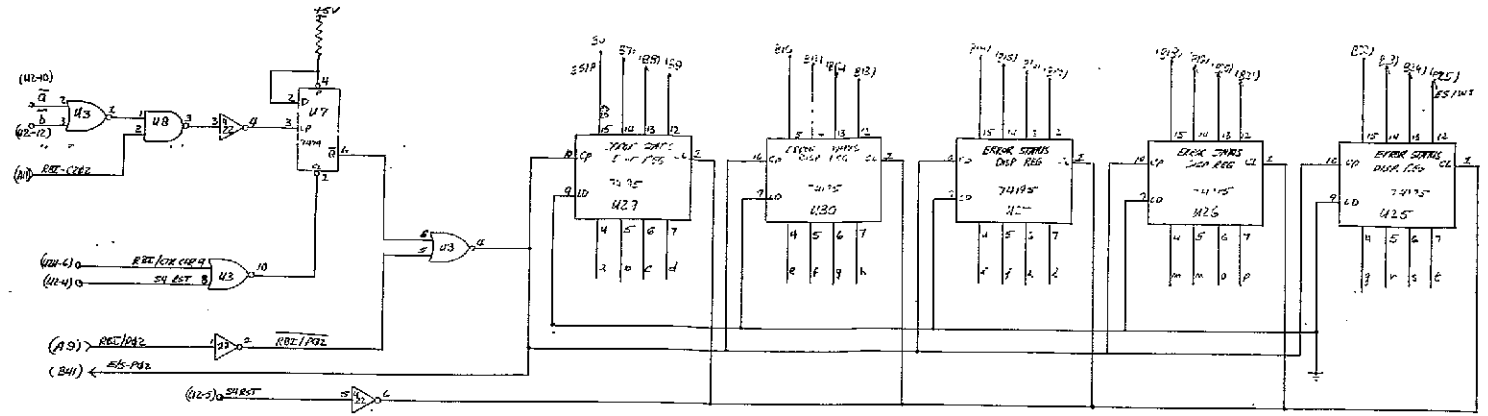
BLANK POSITION - "5"

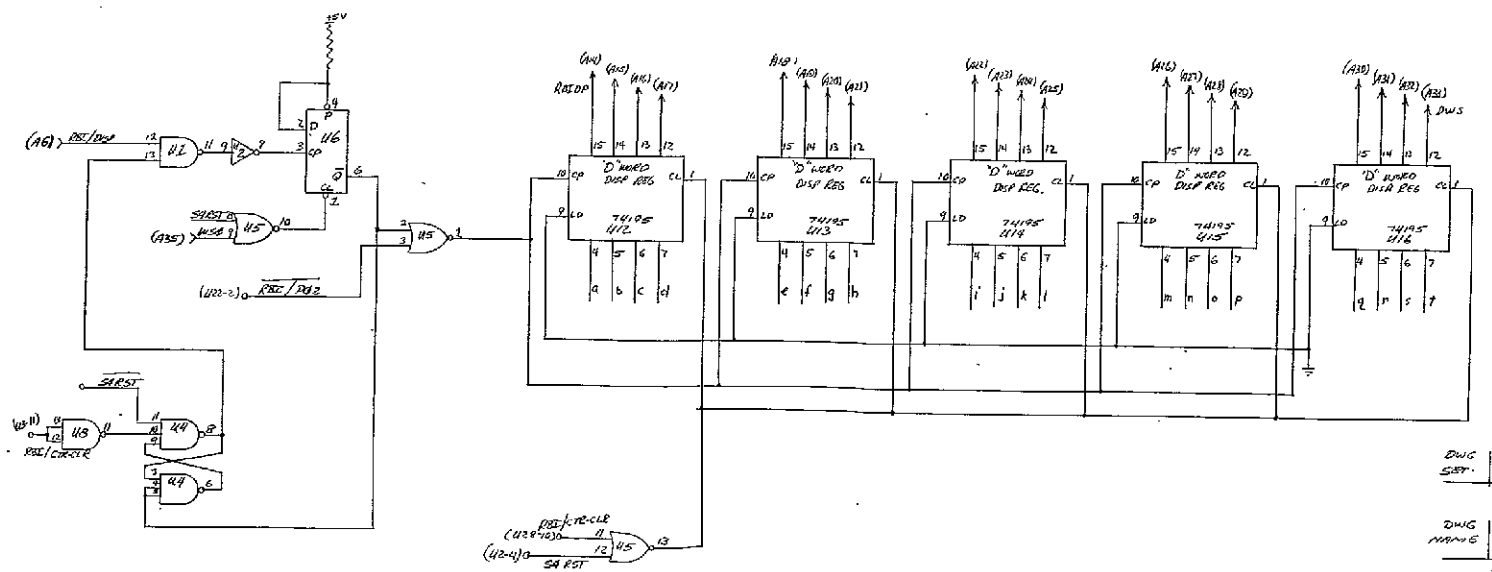


(55a)

BOARD POSITION: (55) (0)

8-15-74
9-5-74
9-20-74
10-7-74
1-31-75





DWG SET: DE4 TEST SET - TCU GROUP B

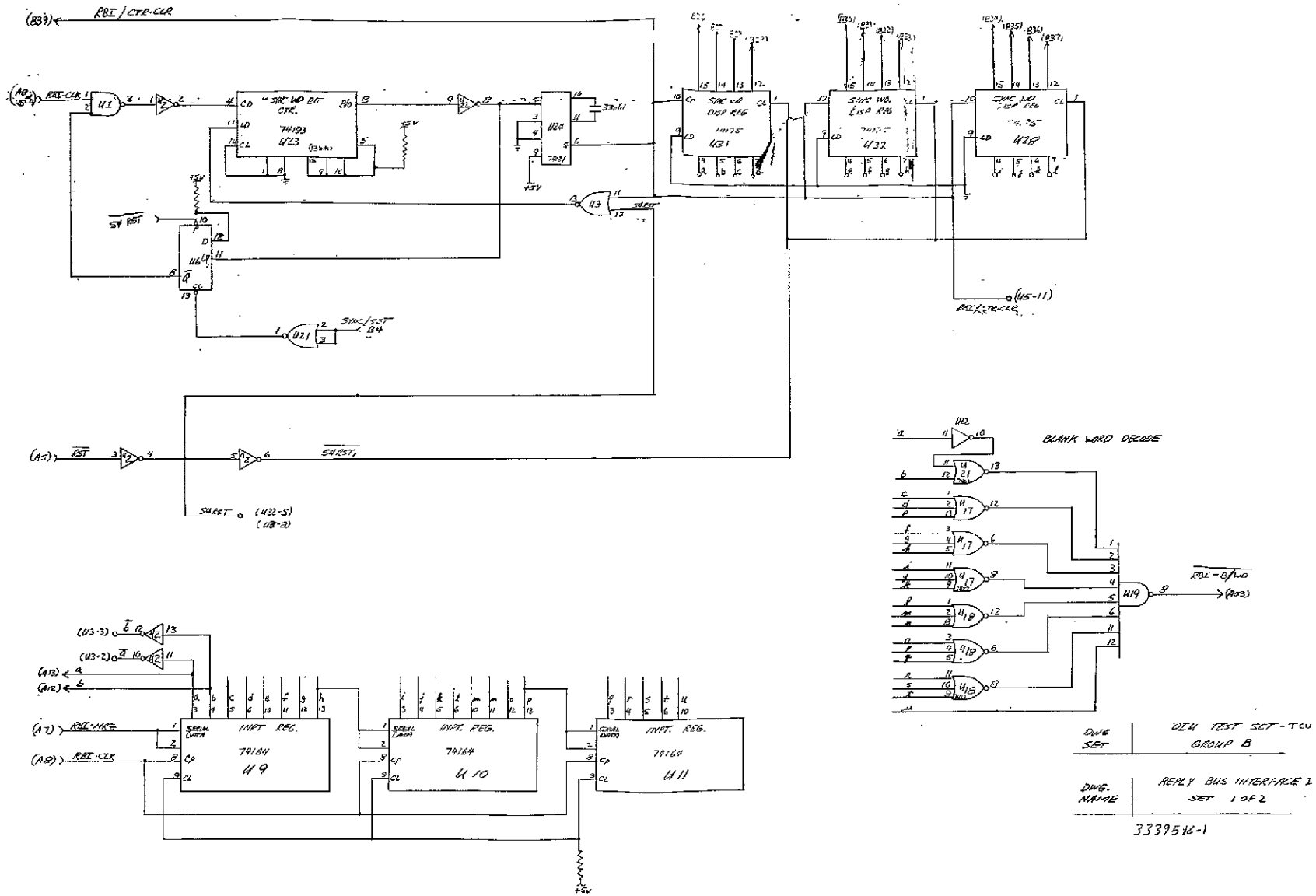
DWG NAME: REPLY BUS INTERFACE 1 SET 1 OF 2

3339516-2

(54-b)

BOARD POSITION : 54b

8-16-75
1-31-75



DWG SET: DLA TEST SET - TCU GROUP B

DWG. NAME: ARMY BUS INTERFACE 1 SET 1 OF 2

3339516-1

(54 a)

BOARD POSITION : 54 a

8-16-74

1-31-75

DATA MANAGEMENT SYSTEM

CIU AND DIU

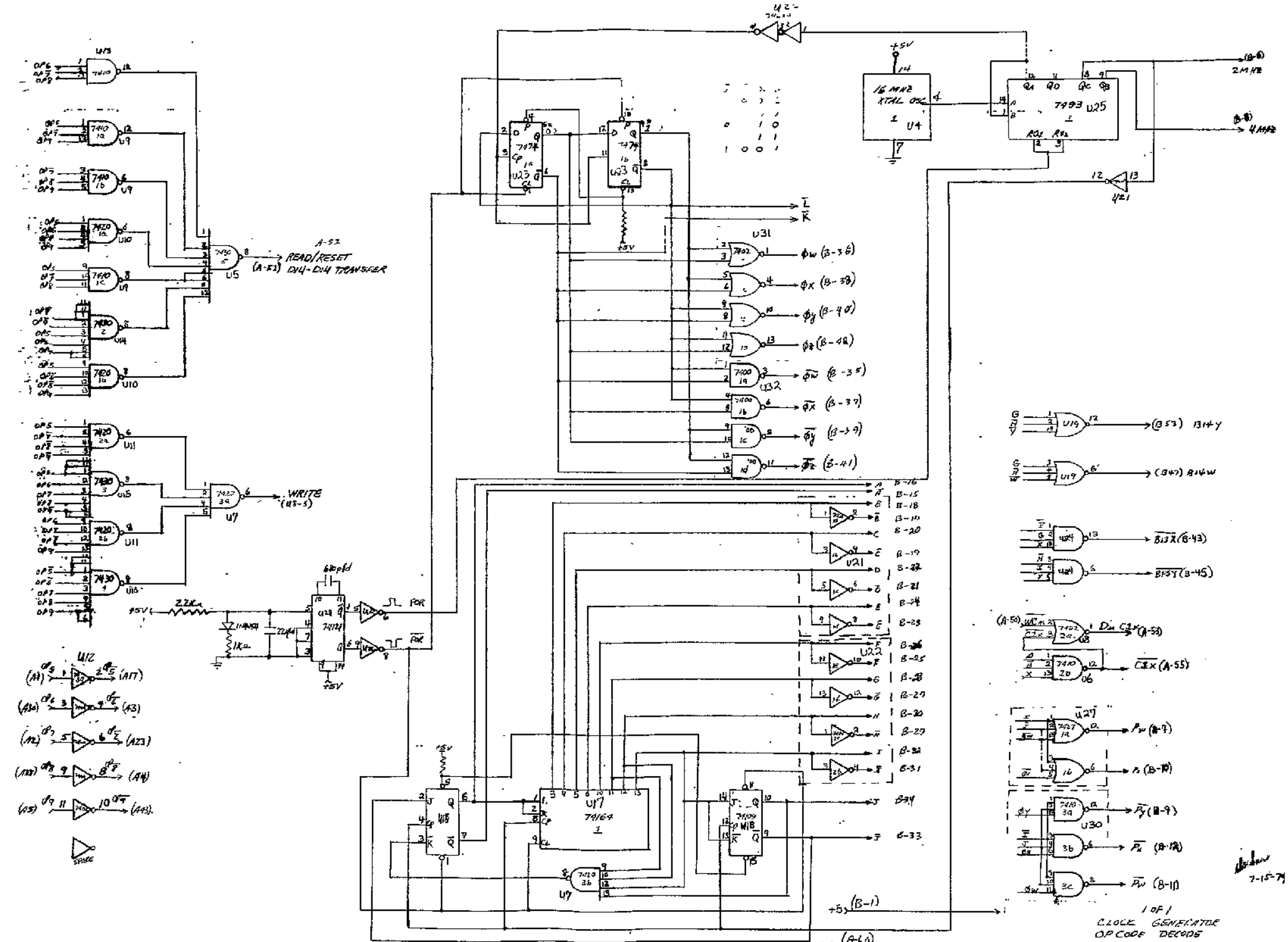
FINAL TECHNICAL REPORT

APPENDIX A

DIU TEST SET SCHEMATICS

PREPARED FOR
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GEORGE C. MARSHALL SPACE FLIGHT CENTER
UNDER CONTRACT
NAS8-31443

PREPARED BY
SCI SYSTEMS, INC.
FEBRUARY, 1976



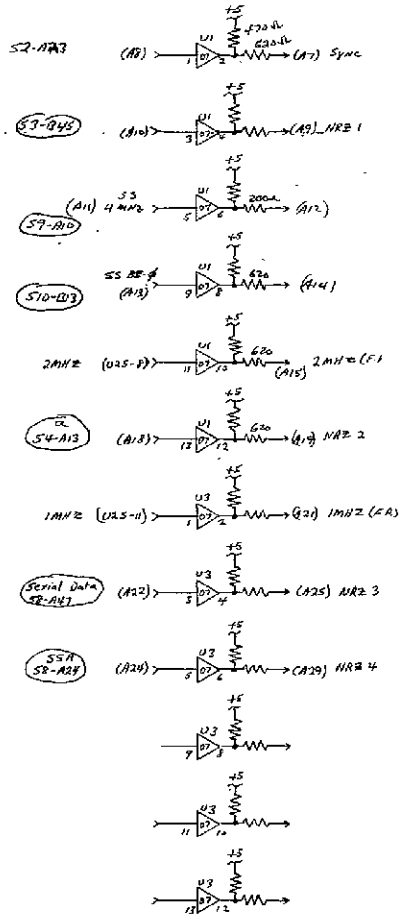
(S1A)

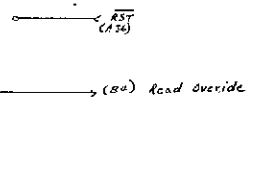
TCU

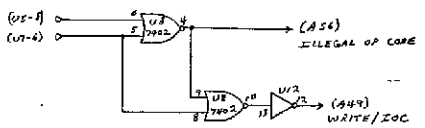
DWG SET	DIU TEST SET GROUP A	DWG NAME	TEST SYNTHESIS TIMING NUMBER 1 OF 2	3339510-1

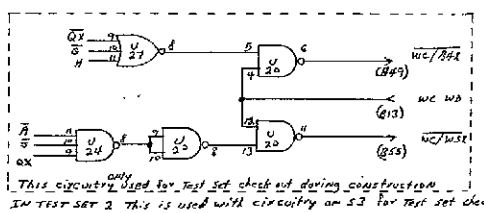
CARD SLOT # 1-A

Front Panel Test Point Buffers

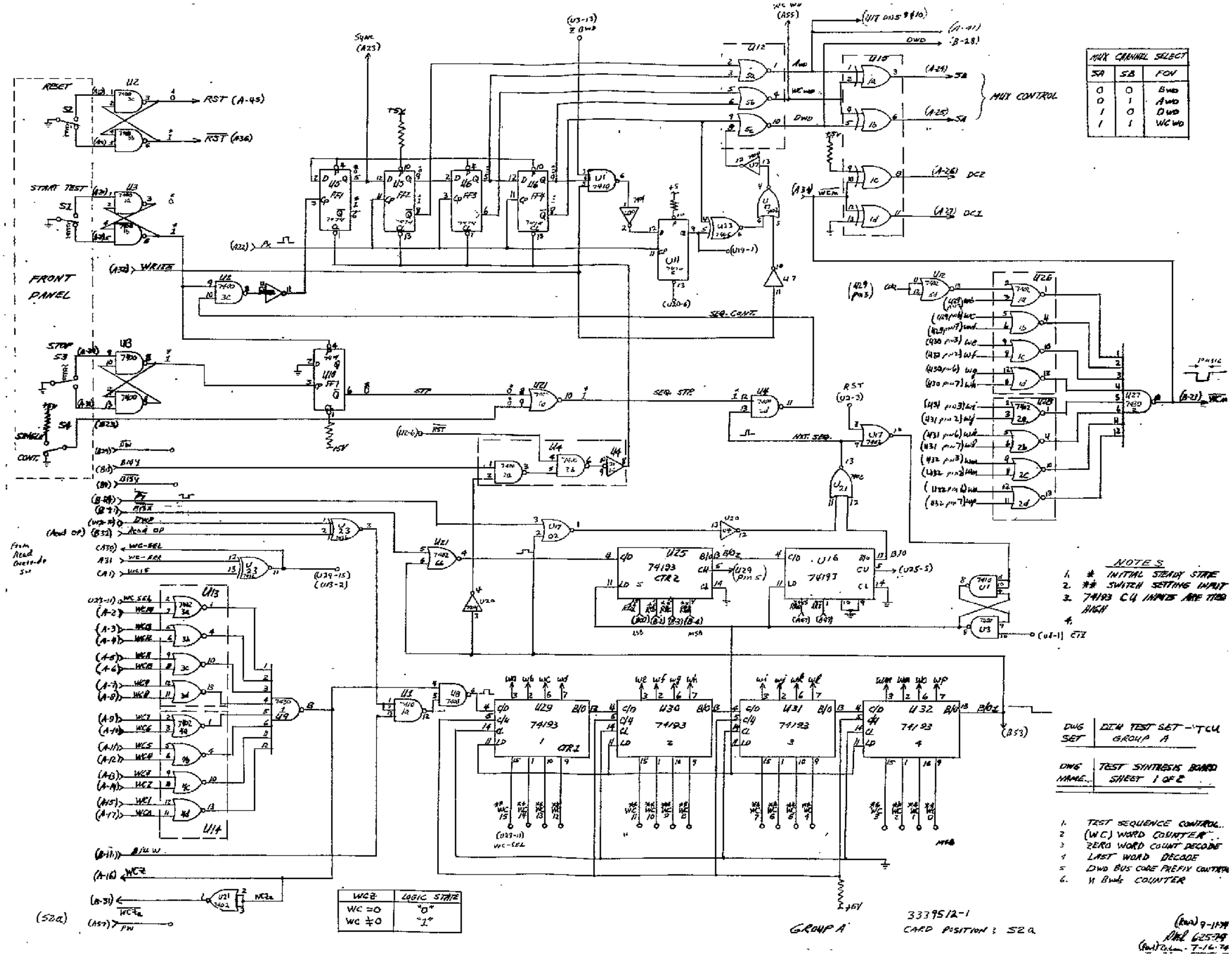




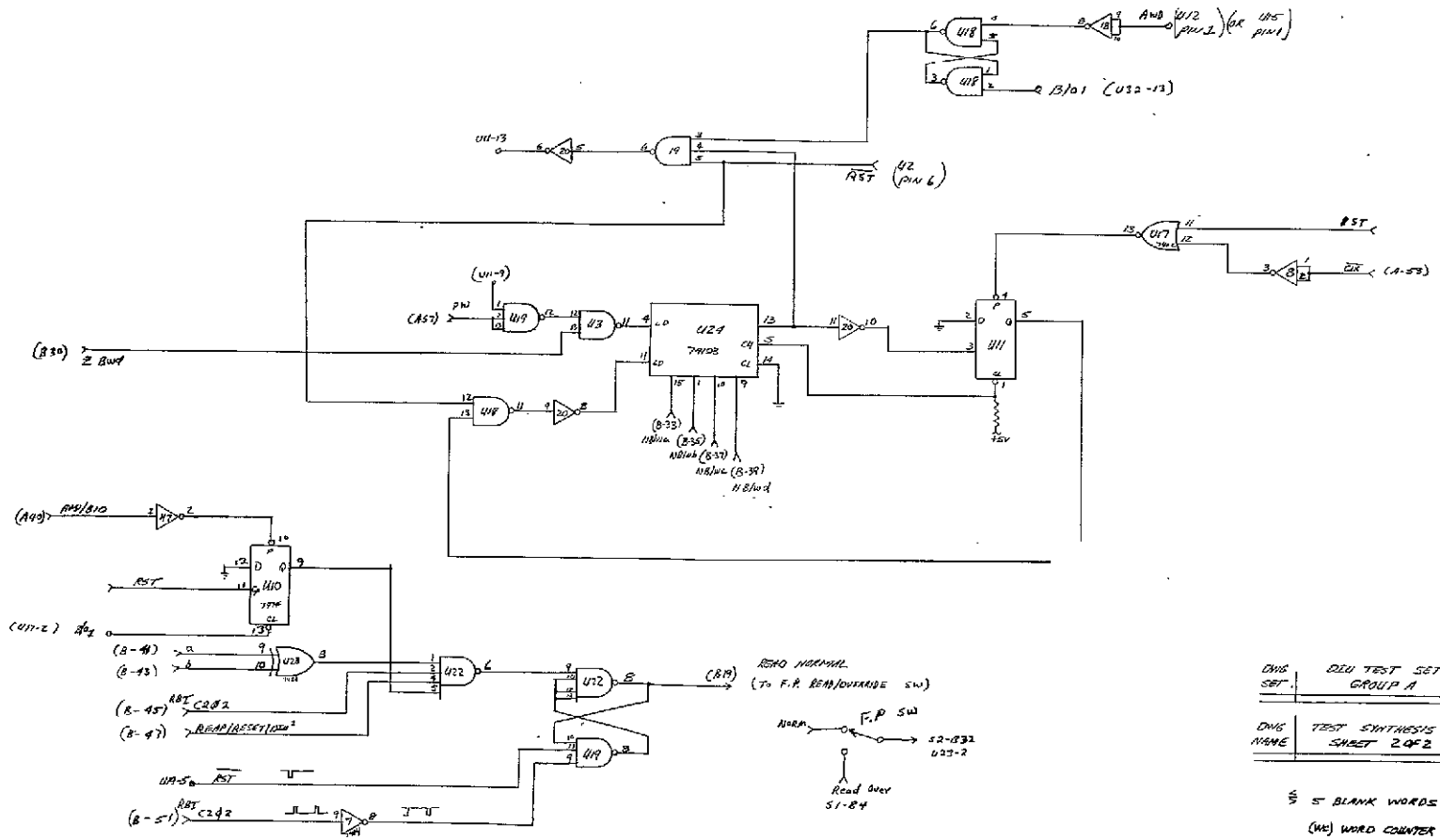




(5/b)



RESET
START TEST
FRONT PANEL
STOP S3
SINGLE
CONT.
RST (A-45)
WRITE
SEQ. CONT.
SEQ. STR
NXT. SEQ.
MUX CHANNEL SELECT
SA | SB | FCN
0 | 0 | Bwd
0 | 1 | Awd
1 | 0 | Dwd
1 | 1 | WCwd
MUX CONTROL
DC2
DC1
WCZ | LOGIC STATE
WC = 0 | "0"
WC ≠ 0 | "1"
NOTES
1. * INITIAL STEADY STATE
2. ** SWITCH SETTING INPUT
3. 74193 CU INPUTS ARE TIED HIGH
4.
DWG SET | DIW TEST SET - TCU GROUP A
DWG NAME | TEST SYNTHESIS BOARD SHEET 1 OF 2
1. TEST SEQUENCE CONTROL
2. (WC) WORD COUNTER
3. ZERO WORD COUNT DECODE
4. LAST WORD DECODE
5. Dwd BUS CODE PREFIX COUNTER
6. N Bwds COUNTER
333951Z-1
CARD POSITION : 52a
GROUP A
(52a)



DWG SET.	DEU TEST SET - TC4 GROUP A
DWG NAME	TEST SYNTHESIS BOARD SHEET 2 OF 2

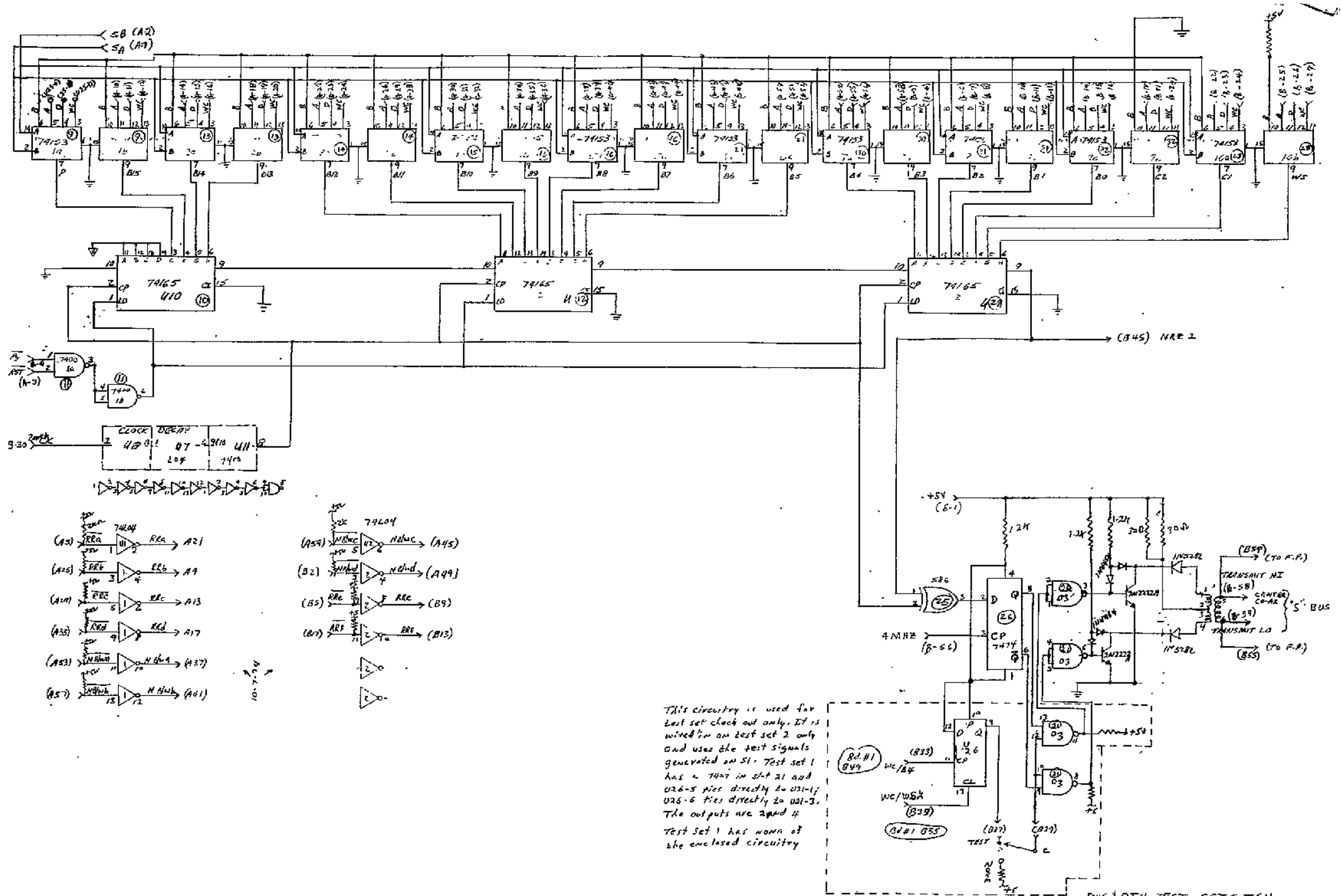
S = 5 BLANK WORDS SYNTHESIS

(WC) WORD COUNTER DECODE

(52-6)

3339512-2
Group A - 52b

9-10-74
DSW

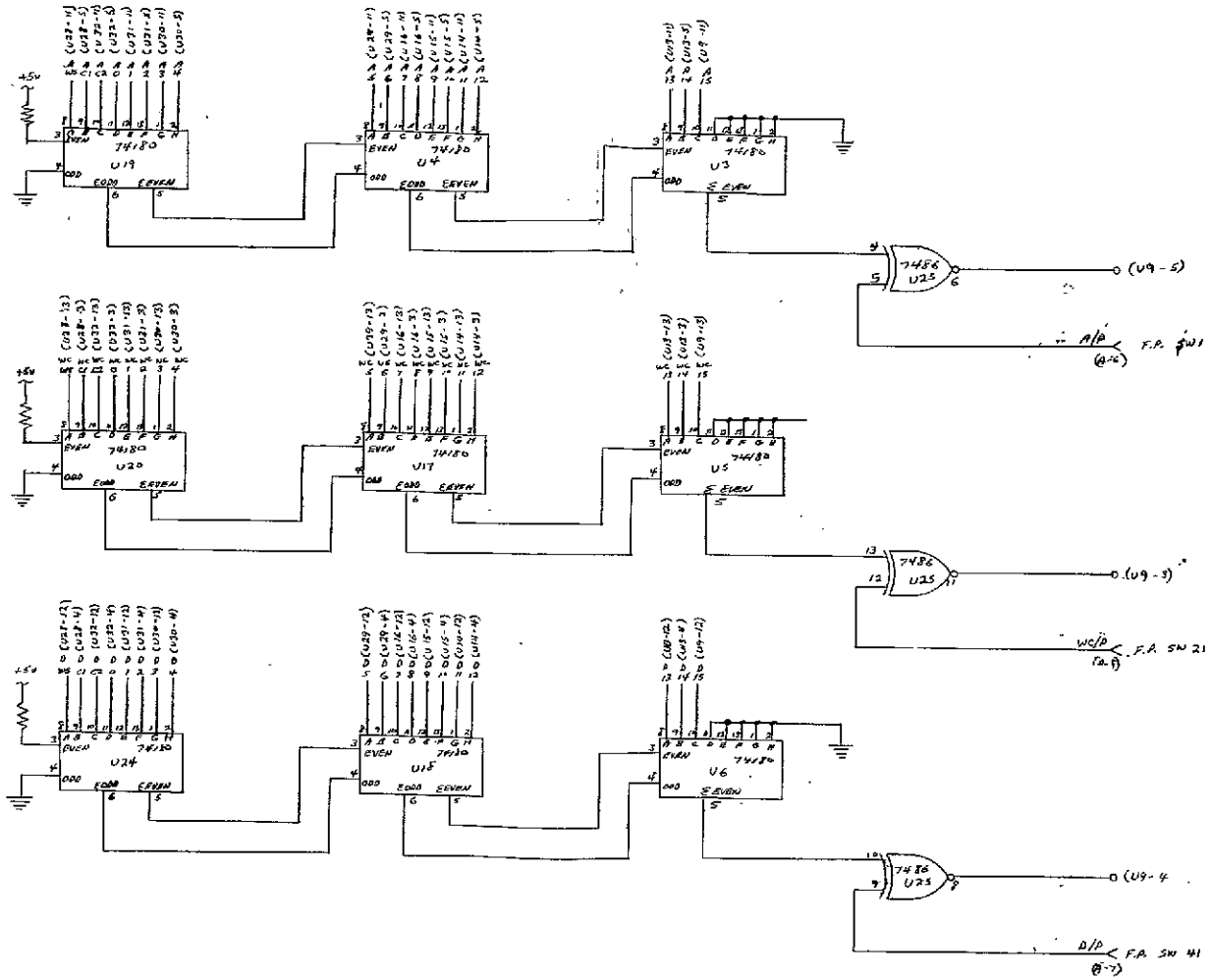


DWG. SET	DIU TEST SET - TCU GROUP A
DWG NAME	"S" BUS INTERFACE SHEET 1 OF 1

WORD MUX
OUTPUT REGISTER
NRZ/BI-Φ CONVERTER
TRANSMITTER

12-10-74
7-23-74
7-1-74
10-7-74

333951X-1 GROUP A
CARD POSITION: SLOT 3 (S3)a



PARITY GENERATOR

536

SLOT 36 3339514-2

1-15-75
QRSm

DATA MANAGEMENT SYSTEM

DIU TEST SYSTEM

FINAL TECHNICAL REPORT

(NASA-CR-144195) DATA MANAGEMENT SYSTEM DIU TEST SYSTEM Final Technical Report (SCI Systems, Inc., Huntsville, Ala.) 92 p HC $5.00 CSCL 09B

N76-18805

Unclas
G3/60 20089

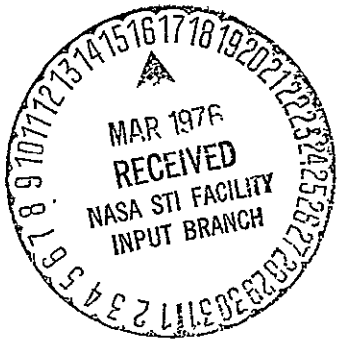
PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

GEORGE C. MARSHALL SPACE FLIGHT CENTER

UNDER CONTRACT

NAS8-31443



PREPARED BY

SCI SYSTEMS, INC.

FEBRUARY, 1976

SCI SYSTEMS, INC.

DATA MANAGEMENT SYSTEM
DIU TEST SYSTEM
FINAL TECHNICAL REPORT

PREPARED FOR
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GEORGE C. MARSHALL SPACE FLIGHT CENTER
UNDER CONTRACT
NAS8-31443

PREPARED BY
SCI SYSTEMS, INC.
FEBRUARY, 1976

TABLE OF CONTENTS

1.0 INTRODUCTION

The information contained in this document detailing the functions of the DIU Test System constitutes the Final Technical Report for NASA-MSFC Contract NAS8-31443.

Section 2 and 3 present functional and operational descriptions of the Test Control Unit (TCU), Analog Stimulus Panel (A-STP), Discrete Stimulus Panel (D-STP) and the Precision Source. The TCU is presented in Section 2 and the Stimulus Panel, comprised of the three separate sections, is described in Section 3.

In Section 4 the internal operation of the units under discussion are presented in terms of block diagram level descriptions. These descriptions are at a level that an engineer skilled in electronic deciplines of the hardware could use them as a guide for employing the appropriate unit schematics (presented in Appendix A), drawings, listings and procedures to make repairs or modifications. The mechanical configuration is defined and illustrated to provide card and component location for modification or repair. The unit level interfaces are mirror images of the DIU interfaces and are described in the Final Technical Report for NASA-MSFC contract NAS8-29155.

2.0 DIU TEST CONTROL UNIT (TCU) CONTROL AND DISPLAY DESCRIPTION

2.1 INTRODUCTION

The DIU TEST CONTROL UNIT (TCU) performs two major functions in the testing of a DIU. It emulates the CIU Transmit/Reply interface and the RI/RO Subsystem Transmit/Reply interface.

The TCU is subdivided into the following areas:

(1) SUPERVISORY BUS CONTROL

Word Select Control

A - Word
WC - Word
D - Word

Sequence Rate Control

Number of Blank Words Control

Instruction Sequence Control

Reset
Reply Auto/Normal
Continuous/Single
Start
Stop

WC Error/Normal Control

Operational Error Display

Illegal OP Code
Word Count 0

(2) REPLY BUS DISPLAY

DIU Reply Display

Sync-Word

D-Word
Error Status - Word
B-Word

D Word Select Control

(3) RI/RO CONTROL/DISPLAY

Data Input Control

Error Status Control

Subsystem D Word Select Control

Clock Select Control

Clock Enable Display

Reply/No Reply Control

Data Out Display

(4) MONITORING FUNCTIONS

Digital Multimeter

System Function Test Points

Power Supply Test Points

(5) POWER CONTROL

System Power Control/Display

DIU Power Control

This document describes the function of these controls and displays. Reference should be made to Figure 2.1-1 which identifies the location of each control and display.

2.2 SUPERVISORY BUS CONTROL

This section of the TCU controls the information and format of the emulated CIU transmit signals on the Supervisory Bus.

2.2.1 Word Select Control

The Supervisory Bus information consists of three words that are controlable from the TCU.

2.2.1.1 A-Word (Address Word) - 20 Bit Switches

2.2.1.1.1 Prefix Bits (WS, C1 and C2 Bits)

WS, C1 and C2 switches constitute the Sync bit and bus code prefix bits respectively. All word sync (WS) bits must be logical "1"s to be valid. This applies to "A" words, "WC" words, "D" words and "Blank" words. Bus code prefix bits C1 and C2 must be logical "1"s for an "A" word. Any of these three switches (WS, C1, or C2) a logical "0" invalidates the "A" word command and a DIU would not recognize the message. This means that a DIU would remain reset awaiting a proper "A" word command.

2.2.1.1.2 DIU Address Bits (Bits 0 thru 4)

Bits 0 through 4 are DIU address switches and are used to select one of 32 possible DIU's. They are binary weighted with Bit 4 beign the Least Significant Bit (LSB).

The DIU address select thumbwheel is an octal switch, therefore the binary address bits programmed by the TCU and the DIU Address Switch must agree as follows to ensure DIU recognition at its address.

TCU "A" WORD SWITCH					DIU ADDRESS SWITCH	
Binary					Decimal	Octal
B0	B1	B2	B3	B4		
0	0	0	0	0	0	00
0	0	0	0	1	1	01
0	0	0	1	0	2	02
0	0	0	1	1	3	03
0	0	1	0	0	4	04
0	0	1	0	1	5	05
0	0	1	1	0	6	06
0	0	1	1	1	7	07
0	1	0	0	0	8	10
0	1	0	0	1	9	11
0	1	0	1	0	10	12
0	1	0	1	1	11	13
0	1	1	0	0	12	14
0	1	1	0	1	13	15
0	1	1	1	0	14	16
0	1	1	1	1	15	17
1	0	0	0	0	16	20
		↓			↓	↓
1	1	0	0	0	24	30
		↓			↓	↓
1	1	1	1	1	31	37

2.2.1.1.3 OP Code Bits (Bits 5 thru 9)

These are the "OP Code" switches that instruct the addressed DIU which program is to be performed. Below are the 5 bit binary instructions to be used. All other Op Codes are invalid and will illuminate the Invalid Op Code (IOC) LED located on the TCU front panel (Figure 2.1-1).

	TCU "A WORD" BITS				
	B5	B6	B7	B8	B9
WRITE DO's	1	1	0	0	0
WRITE DI MONITOR CONTROL	1	0	0	0	0
WRITE AI DELTAS (AIØ-AI63)	0	1	1	0	1
WRITE AI DELTAS (AI64-AI127)	1	1	1	0	1
WRITE AO's	1	1	1	1	0
WRITE RO	0	0	1	1	1
READ RI	0	0	0	1	1
READ ERROR STATUS	0	1	0	1	0
READ AI DELTAS (AIØ-AI63)	0	1	0	1	1
READ AI DELTAS (AI64-AI127)	1	1	0	1	1
READ AI EXCEEDING DELTAS	1	1	1	0	0
READ AI's	1	1	0	1	0
READ DO STATUS	1	1	0	0	1
READ DI MONITOR CONTROL	1	0	0	1	1
READ DI CHANGE	1	0	0	1	0
READ DI's	1	0	0	0	1
DIU TO DIU TRANSFER	1	0	1	0	1
RESET	1	1	1	1	1

2.2.1.1.4 Channel Address Bits (Bits 10 thru 15)

The channel address switches select a 6 bit binary channel command. Bit 15 is the least significant bit (LSB). Each DIU shall be able to control its DO's DI's, AO's, AI's, and RI/RO's by the channel address.

EXAMPLE: RI/RO --------- Select one of eight possible sub system channels. The codes are:

Binary						Octal/Decimal
B10	B11	B12	B13	B14	B15	
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
0	0	0	1	0	0	4
0	0	0	1	0	1	5
0	0	0	1	1	0	6
0	0	0	1	1	1	7

NOTE: The "Clock Sel" switch in the TCU RI/RO section (Figure 2.1-1) will determine which of the above channels will be received by the sub system (RI/RO section). This switch (thumbwheel) is an octal switch, however digits 0 through 7 are the same in octal and decimal.

2.2.1.1.5 Parity Bit (P Bit)

The parity switches for all CIU Type words enter either "odd" or "even" parity depending on the switch position. Odd parity is the correct parity and is entered with the parity switch in the down or "0" position. To check DIU parity error detection capabilities, "even" parity is entered by the ("1") position.

2.2.1.2 WC-Word (Word Count Word) - 20 Bit Switches

2.2.1.2.1 Prefix Bits (WS, C1 and C2 Bits)

WS valid is a logical "1" as for the "A" words. Bus code prefix bits will be C1=1 and C2=1 for a write operation and C1=0 and C2=1 for a read operation. The "01" prefix indicates an "end of message" meaning the words to follow will be blank words. The "11" means that data will follow.

2.2.1.2.2 Word Count Bits (Bits 0 thru 15)

These are binary word count bits which determine the magnitude of the message field. Bit 0 is the MSB(2^{15} = 32768) and Bit 15 is the LSB (2^{0}=1).

2.2.1.2.3 Parity Bit (P Bit)

The parity bit is the same as for the "A word".

2.2.1.3 D Word (Data Word) 20 Bit Switches

2.2.1.3.1 Prefix Bits (WS, C1 and C2 Bits) for Data Entered in a write operation.

The WS bit is the same as for A & WC words. The C1 and C2 bus code prefix bits are "10" and "01" for D words with more to follow and D word end of message respectively. The switches do not control these bits. They are automatically entered properly.

2.2.1.3.2 Data Bits (Bits 0 thru 15)

These are the Date message bits and can be set to any desired pattern consistent with the write operation being conducted.

2.2.1.3.3 Parity Bit (P Bit)

Same as "A" and "WC" words.

2.2.2 Sequence Rate Control (2 octal thumbwheel switches)

This set of 2 octal thumbwheel switches can be employed to insert up to 64 blank words between message sequences. A minimum of 1 blank word is required, One blank word will exist when the switches are set to 00. The number of blank words is 1 more than the decimal conversion of the octal number set into the switches. Using the maximum setting as an example:

77 - Switch setting in Octal
63 - Decimal Conversion
+1 - Correction Constant
64 - Number of Blank Words

2.2.3 Number of Blank Words Control (1 Decimal Thumbwheel Switch)

This is a decimal (BCD coded) thumbwheel switch. Its function is to insert blank words between Data Words (D-Words) during a Write Operation. It provides a means of testing a DIU's ability to identify more than the 5 blank words between Data Words. The number of blank words can be controlled from 0 to 9. When entering a number from 0, the TCU must be reset and re-started to initialize the logic properly. Changing from any number other than 0 this is not required.

2.2.4 Instruction Sequence Control (5 Function Switches)

This is a group of 5 function switches used to control bus operations as defined in the paragraphs to follow.

2.2.4.1 Reset (Momentary Toggle Type Switch)

This switch resets the TCU when depressed. Counters and command logic in the TCU are initialized which causes blank words to be transmitted on the S-Bus until a program is initiated by the Start Switch.

2.2.4.2 Reply AUTO/NORM (Toggle Switch)

This switch is used for Read Operations. In the AUTO position the TCU Word Counter is decremented each word time after the WC-Word. This eliminates any dependancy on returned data from the DIU. In the NORM position the operation of the TCU will be dependent on data returning from the DIU. For Read RI operations this switch should be in the NORM position

to prevent over lapping replays from the DIU with the next message instruction.

2.2.4.3 CONT/SINGLE (Toggle Switch)

This switch programs the TCU for either single messages or multiple (continuous) message operation. Most basic test are conducted with the switch in the CONT position.

2.2.4.4 START (Momentary Toggle Type Switch)

This switch controls the start of each test program. When the CONT/SINGLE Switch is in SINGLE Position the reset switch isn't need to reset the TCU. Simply depress and release the start switch to send the next message. In any mode the start of any test is begun by depressing and releasing this switch.

2.2.4.5 STOP (Momentary Toggle Type Switch)

Depressing and releasing the stop switch will terminate any message at the end of its transmission. In single mode this switch isn't necessary. It will not terminate a message prior to end of message.

2.2.5 WC ERR/NORM Control (Toggle Function Switch)

This switch is the word count error control and is used for word count error checking. In the "ERR" position it will induce a word count error by modifying the "WC WORD" word count field. In a write operation this means the number of Data words issued and the number of Data words expected (the number defined by the word count field) will be in variance. In the NORM position there is no alternation of the expected data words.

2.2.6 Operational Error Displays

Two flags to indicate operational errors have been included in the TCU. They are illegal OP Code entered (IOC) and word count of zero (W/CO) entered. The flags are to allert the operator to errors.

2.2.6.1 Illegal OP Code - IOC (LED Bit Display)

This indicator is lit when an illegal OP Code has been entered by the operator. When an illegal OP Code is entered the TCU will operate as if a write command had been programmed. The IOC flag will be illuminated but the TCU will continue transmitting messages with the "A" word containing the bogus OP Code. The responding DIU should set the "OP Code" flag in the returned error status word. See figure 2.1-1.

2.2.6.2 Word Count of 0 - W/C = 0 (LED Bit Display)

A word count of zero (W/C = 0) is a non-defined operation and should be avoided. If W/C=0 is entered by the operator this indicator will be lit.

2.3.0 REPLY BUS DISPLAY

CIU receive data are presented by the "DIU REPLY" led indicators. This section consists of a returned 12 bit sync word, data word display (used in read operations), error status word and first blank word received flags. A D word select control is used to select a specific D-Word to display from the message.

2.3.1 DIU Reply Display (LED Bit Display)

2.3.1.1 Sync - Word (12 LED's)

This group of 12 LED's display a fixed 6 bit code (111101), 5 bits that displays the returned DIU (wired) address, and a parity bit. The odd parity is only for the 5 bit DIU address and does not include the 6 bit fixed sync code.

2.3.1.2 D-Word (20 LED's)

Displays the prefix (WS, C1 and C2), information (Bits 0 thru 15) and Parity bit.

2.3.1.3 Error Status - Word (20 LED's)

The error status word will display returned errors and a DIU DIU transfer flag (bit 0). The "DIU TRANS" indicator will be on for a valid trnasfer. This display includes the prefix bits (WS, C1 and C2), error and flag information (bits 0-15) and parity bits.

2.3.1.4 B-Word (1 LED)

The "B Word" flag indicated that the first word received when the reply bus was activated was a blank word.

2.3.2 D-Word Select Control (3 Octal Thumbwheel Switches)

The "D word sel" thumbwheels will determine which "D" word in a data stream will be displayed. They are octal switches and are compared with the data received to determine the "D" word to be displayed. When the "D word sel" and word count are the same "D" word end of message should be displayed. This is verified by the bus code prefix bits C1 and C2 which change from "10" to "01"

2.4 RI/RO CONTROL/DISPLAY

Functions in the RI/RO section of the TCU are similar to those for the CIU interface section. Controls are provided to supply the DIU RI interface proper inputs to exercise and test the RI function. Controls and Displays are provided to verify and test the DIU RO outputs.

A read RI OP Code of 00011 will present data to the Subsystem/DIU interface and is programmed by the DATA IN and ERROR STATUS switches.

A write RO OP Code of 00111 will command the DIU to supply data to the TCU to be displayed by the DATA OUT indicators.

2.4.1 Data In Control (20 Bit Switches)

These switches are the same as "D word" switches in the CIU interface section. Parity will be entered automatically either "even" or "odd" as described in previous sections.

2.4.2 Error Status Control (8 bit switches)

These 8 switches provide a simulated sub system error status word. The sub system saved error status bits are labeled 12, 13, 14 and 15 to match their positions in the DIU error status word (see fig. 1,RI/RO and DIU REPLY sections). They are programmed manually to simulate errors. Parity is not entered automatically and must be determined by the 7 preceeding error status switch positions. WS, C1 and C2 bits shall be 111 for proper operation.

2.4.3 Subsystem D Word Select Control (3 Octal Thumbwheel Switches)

As with "D word" display in the "DIU REPLY" section, "SUB SYS D WORD SEL"

thumbwheel switches will select the data word, received from the DIU, to be displayed.

2.4.4 Clock Select Control (1 Octal Thumbwheel Switch)

Selects the RI/RO channel (1 of 8) to be tested by the TCU.

2.4.5 Clock Enable Display (8 LED Displays)

These leds correspond to the "clock sel" switch. They display which channel is to be selected. For proper operation in either Read RI or write RO the "clock sel" switch, "A" word channel address switches and "clock enable" indicators must agree.

The information presented to the DIU will be returned to the TCU via the reply bus and will be displayed in the "DIU REPLY" display section. Therefore, changing bits in the RI/RO section "DATA IN" and "ERROR STATUS", will be mapped back into the "DIU REPLY" display section.

2.4.6 Reply/No Reply Control (1 toggle switch)

The REPLY/NO REPLY Switch will determine whether the RI/RO section will respond to interrogation by a DIU. It is used to check Sub System response error condition. This is bit 10 in the returned error status word.

2.4.7 Data Output Display (20 LED Displays)

A "WRITE RO" OP Code (00111) will direct the addressed DIU to pass the Data written into it, by the TCU, on to the sub system (RI/RO) via the RO line. The data will be displayed by the "Data Out" indicators. Changing the "D word" bit pattern in the "word select" section will be mapped back into the TCU "Data Out" indicators. When the word count has been satisfied, an error

status word will be returned to the DIU, and then returned to the TCU "DIU REPLY" indicators.

2.5 MONITORING FUNCTIONS

2.5.1 Digital Multimeter

A digital multimeter is included in the TCU for the purpose of measuring DC volts, AC volts, Resistance, DC Micro Amps and AC Micro Amps. The resistance ranges selectable are: 100Ω, 1KΩ, 10KΩ, 100KΩ, 1MΩ, 10 MΩ. Voltage and Micro Amp ranges are: 1, 10, 100 and 1000. A special 1000 Micro Amp input is required for the last AC or DC Micro Amp range. This is a 31/2 digit decimal display. A ZERO control is included on the front panel.

2.5.2 System Function Test Points (11 TP's)

The following listed test points are provided on the front panel.

SYNC
NRZ 1 (S-Bus)
BI Ø - HI
BI Ø - LO
2 MHZ
NRZ 2 (R-Bus)
1 MHZ
NRZ 3 (RI)
NRZ 4 (RO)
4 MHZ REC (RO)
SS BI Ø OUT

2.5.3 Power Supply Test Points (5 Power TP's and 2 Gnd TP's)

The power test points are for monitoring the power supplies. They are not to be used as sources for auxiliary equipment. The supplies have labled fuses located on the rear panel. Power TP's are: +5V, +5VFP, +12V, -12V and +28V.

2.6 POWER CONTROL

2.6.1 System Power Control/Display (Indicating Switch)

The "System Power" switch is a push button illuminated switch. The lamp is a 5V miniature. To energize the TCU depress and release this switch.

2.6.2 DIU Power Control (3 position toggle switch)

This switch controls the output of the power supply in the TCU that provides power to the DIU being tested. It is a three position switch and it can be changed to test the input voltage requirements of the DIU NORM position outputs +28VDC. The HI position provides 32 VDC and the LO position provides 22VDC. The switch can be changed while the power supply is being loaded by the DIU.

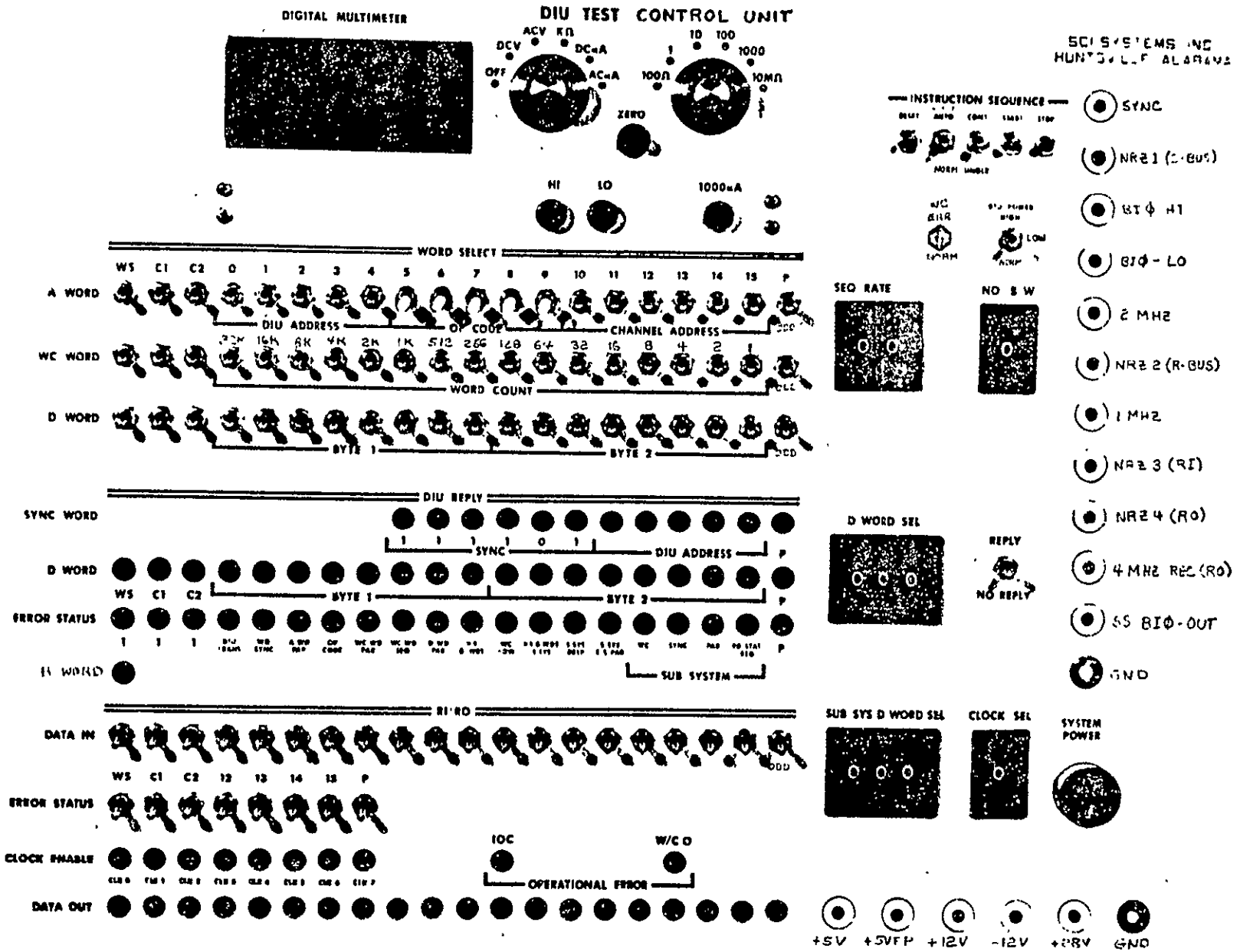


Figure 2.1-1

3.0 DIU STIMULUS PANEL (STP) FUNCTIONAL DESCRIPTION

3.1 INTRODUCTION

The function of the DIU Stimulus Panel (STP) is to provide all of the Stimuli, and loads, required to functionally verify the performance of each of the Discrete and Analog channels under test.

Three separate panels comprise the DIU STP; one each for the Precision Analog Source, Analog functions and Discrete functions. Each function panel has its control switches and test points bracketed to conform to the functional modularity as described in the DIU specification.

The STP when used in conjunction with the Test Control Unit (TCU) completely exercises the DIU under test to the levels set forth in the specification. The DIU Acceptance Test Procedure (ATP) outlines the tests to be conducted using this equipment, and identifies the auxiliary test equipment required.

3.2 DIU ANALOG STIMULUS PANEL/PRECISION POWER SUPPLY

The purpose of the Analog Stimulus Panel is to completely exercise the AI channels of the DIU under test. To ensure proper signal levels are issued a precision, programmable, analog power supply is used for the stimulus of each AI channel.

AI's are selected by 128 toggle switches located on the front panel. The switches are labeled sequentially from 0 through 127 corresponding to the 128 possible AI channels. Additionally, the programming modularity is 8 groups of 16 switches per group, with the first group being designated group 0. Reference should be made to Figures 3.2-1 and 3.2-2 for the location and operation of each control and test point.

To select a particular mode of operation a Stimulus Select switch has been incorporated which allows for Normal, Open (isolation and continuity tests), +32V (overvoltage tests) and -32V (under voltage tests).

For common mode rejection tests the Stimulus Selector is set to the NORMAL position and the Common Mode Switch is set to EXTERNAL, allowing for coupling of the common mode signal into the analog source return. An external source provides the 400 Hz signal, and is coupled via the COMMON MODE INPUTS test points. For all other AI tests the Common Mode switch is set to the ground (GND) position.

To verify channel crosstalk is within limits, bias, or noise, signals are injected into one or more channels with the adajacent channels having normal analog information. The AI Bias Switch in the external position allows the bias to be entered into the selected channels. Crosstalk verification is obtained by monitoring the normal channel's D-word display on the TCU front panel. It should not be affected by the noise on the adjacent channel. For normal AI operation the Bias Switch is set to the GND postion.

AI isolation and continuity tests are accomplished using the CONT/ISOL SELECTOR Switch for group (16 channels) selection, then measurements between switched and unswitched COMM/CH. GND test points are performed. The complete procedure is detailed in the DIU acceptance test procedure, Section 7.2.

The remaining test points (AI INPUTS) allow for the verification of proper output signal levels using a suitable Digital Voltmeter.

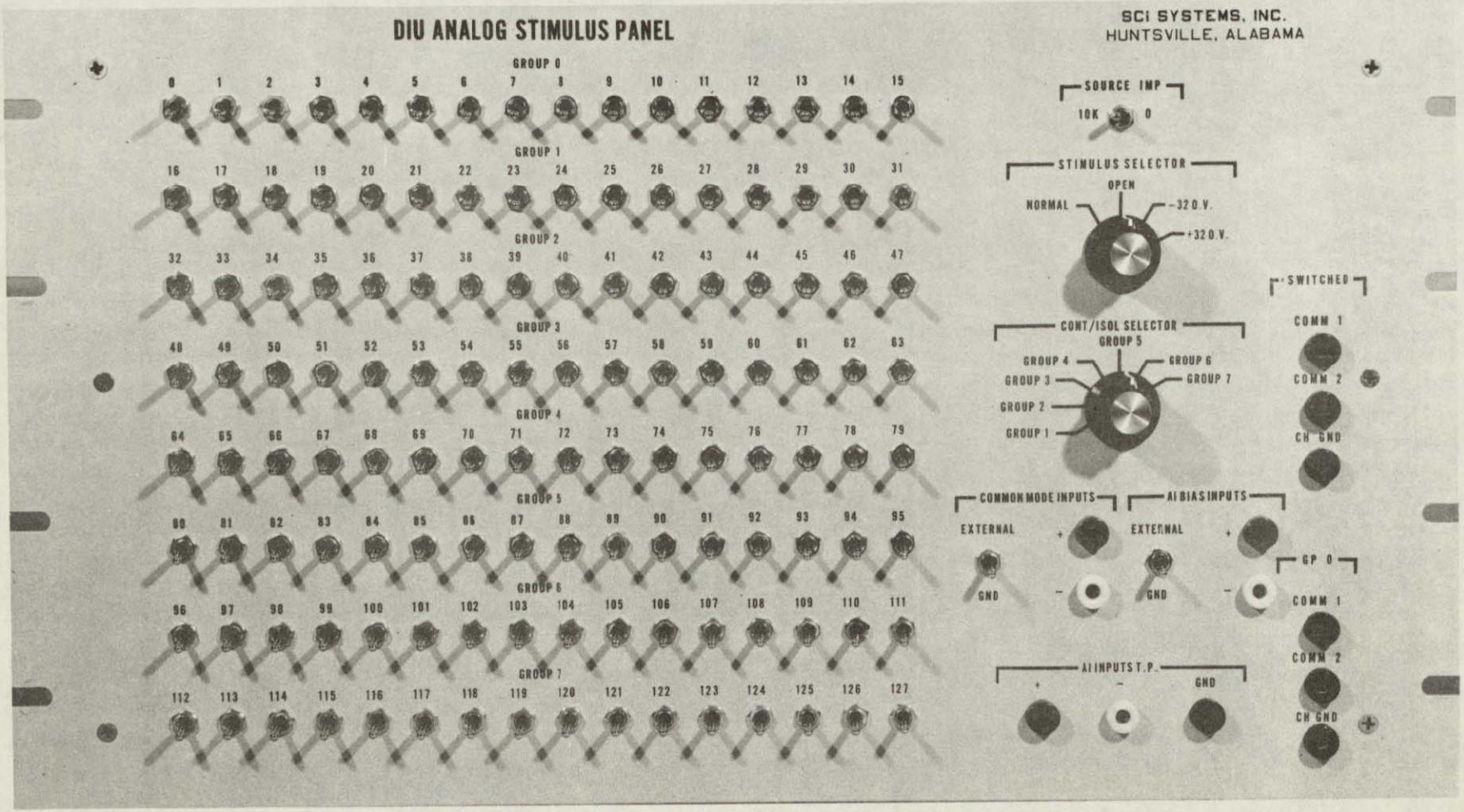


Figure 3.2-1

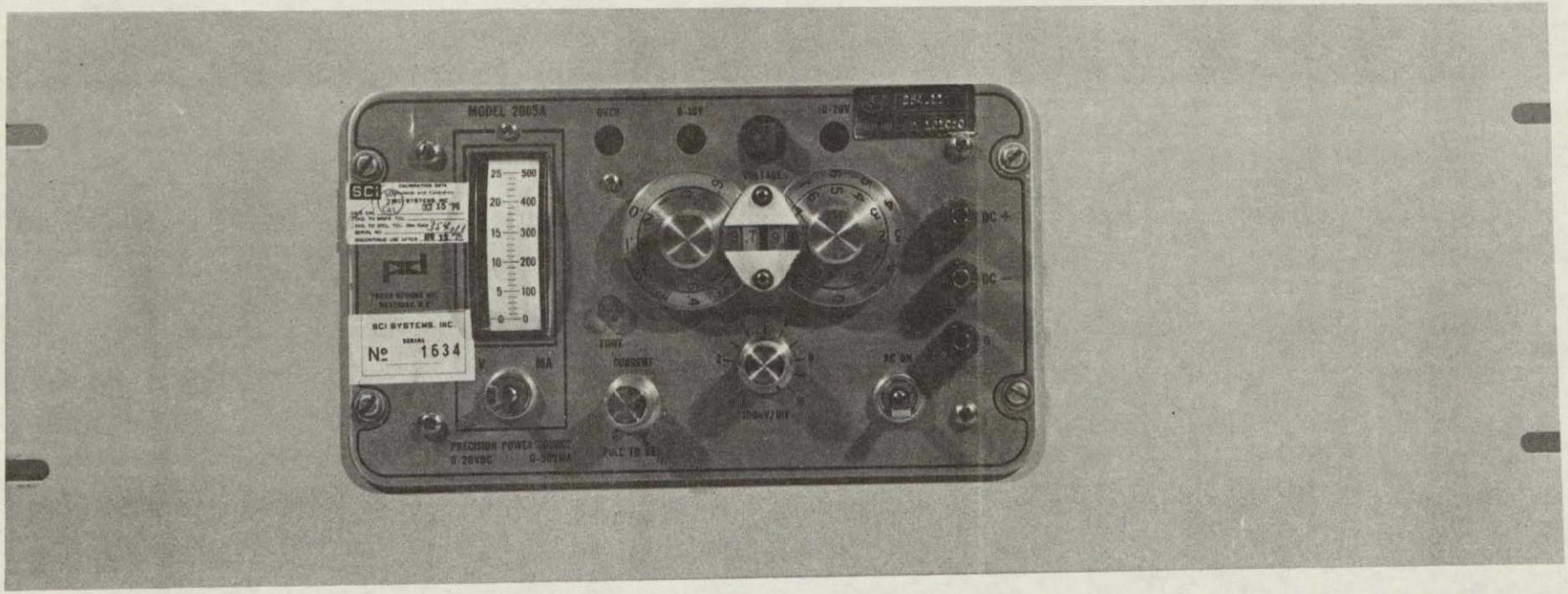


Figure 3.2-2

3.3 DIU DISCRETE STIMULUS PANEL FUNCTIONAL DESCRIPTION

3.3.1 Introduction

Discrete Inputs (DI's), Discrete Outputs (DO's), and Analog Outputs (AO's) are programmed using this panel in conjunction with the TCU. Figure 3.3-1 should be used for reference in determining the location and functional setting of each control switch and test point.

3.3.2 Discrete Input (DI) Discussion

The modularity of the 128 DI's has been defined as being 8 DI words of 16 bits (channels) each. Each word has been assigned a group number sequentially labeled from 0 through 7. The DIU Acceptance Test Procedure (ATP), section 5.1.5, further delineates the words as being HI LEVEL, LO LEVEL or SINK, and when shipped the DIU's had, (1) groups 0, 2, 4 and 6 set as HI LEVELS, (2) groups 1 and 3 set as LO LEVELS, (3) groups 5 and 7 as SINK channels. Before checking DI's ensure the Signal Type Switches (STSW's) for even and odd groups are set to the correct position for the groups under test. The STSW's are labeled HI LEVEL, LO LEVEL and SINK, see Figure 3.3-1. Each group is bit (channel) programmable using the CHANNEL SELECT SWITCHES (CSSW's) which are the 32 toggle switches, 16 each under the DISCRETE INPUTS (EVEN) or (ODD) headings.

DI isolation testing is accomplished in a manner similar to that for AI's described in the proceeding section, section 3.2, using both the even and odd (return, ground and common) test points. See the DIU ATP section 5.2 for the complete procedure. Additionally, the switched return switch (RTSW) is set to the open position for the isolation portion of DI testing and is set to ground for all other tests.

A pulse mode switch has also been incorporated to provide 2 msec pulsed outputs used to verify the performance of the 2 msec transient supression filter on each DIU's DI channel input lines. For all DI tests, excluding filter verification, the PULSE/DC switch (PSW) is set to the DC position.

3.3.3 Discrete Outputs Discussion

The Discrete Outputs (DO's) channel modularity is essentially the same as that of the DI's discussed in section 3.3.2 with the following exceptions, (1) EVEN groups are HIGH level interfaces, and (2) ODD groups are LOW level interfaces. Since there is the possibility of modules being swapped around in the field the strapping sequence could have been altered, therefore, it is extremely important to verify the DO strapping prior to any DO testing. Drawing 3339004 shows the output strapping. Loads presented to the DO interface have been calculated to provide a maximum load of 50 ma. Since loads for 5 volt signal levels would necessarily stress the DO output transistors if 32 volts were applied the voltage source switches will select the correct loads for the source voltage selected. Then once DO modularity (strapping) has been determined be certain the V-supply switch, Figure 3.3-1, is set to the correct position for the DO under test, ie, as preset at the factory only DO's (EVEN) should have the VS VSW set to 32 V. Either EVEN or ODD can be set for +5 V operation without stressing the system.

DO isolation tests are conducted in a manner similiar to that previously stated for AI's and DI's using the ground, common, and channel ground test points plus the Return switches.

Short circuit tests are conducted using the bit (channel) toggle switches located in Figure 3.3-1 under the headings Discrete Outputs (EVEN) or (ODD). For the short circuit testing the following precautions must be adhered to in order to prevent damage to the equipment.

WARNING! (1) Switch only one bit (channel) switch to the ground (up) position at a time, and always return the switch to the normal (down) position prior to shorting the next channel.

(2) Verify DO module strapping prior to testing.

To verify DO outputs from the DIU LED indicators are provided for the groups being tested. The LED's will be on for all DO "1's" being issued to the interface and off for all "0's". In addition the LED's will turn off whenever the output channels are grounded during the short circuit tests.

3.3.4 Analog Output (AO) Discussion

The four Analog Output (AO) channels, A_0 through A_3, are functionally exercised by the TCU AO programming used in conjunction with the loads provided by the Discrete Stimulus Panel (Discrete STP). Each AO channel load is switch programmable to present either the normal 2K ohm resistive load, or a short circuit to the AO interface under test. The four swtiches are grouped under the Analog Outputs heading on the Discrete STP with the test points for each channel directly below the switch.

The test points are used for monitoring via. a suitable Digital Voltmeter each channel during functional testing. For isolation and continuity checks the AO return lines are switched open by the returns open/ground switch. All other tests require the switch to be set to the ground position.

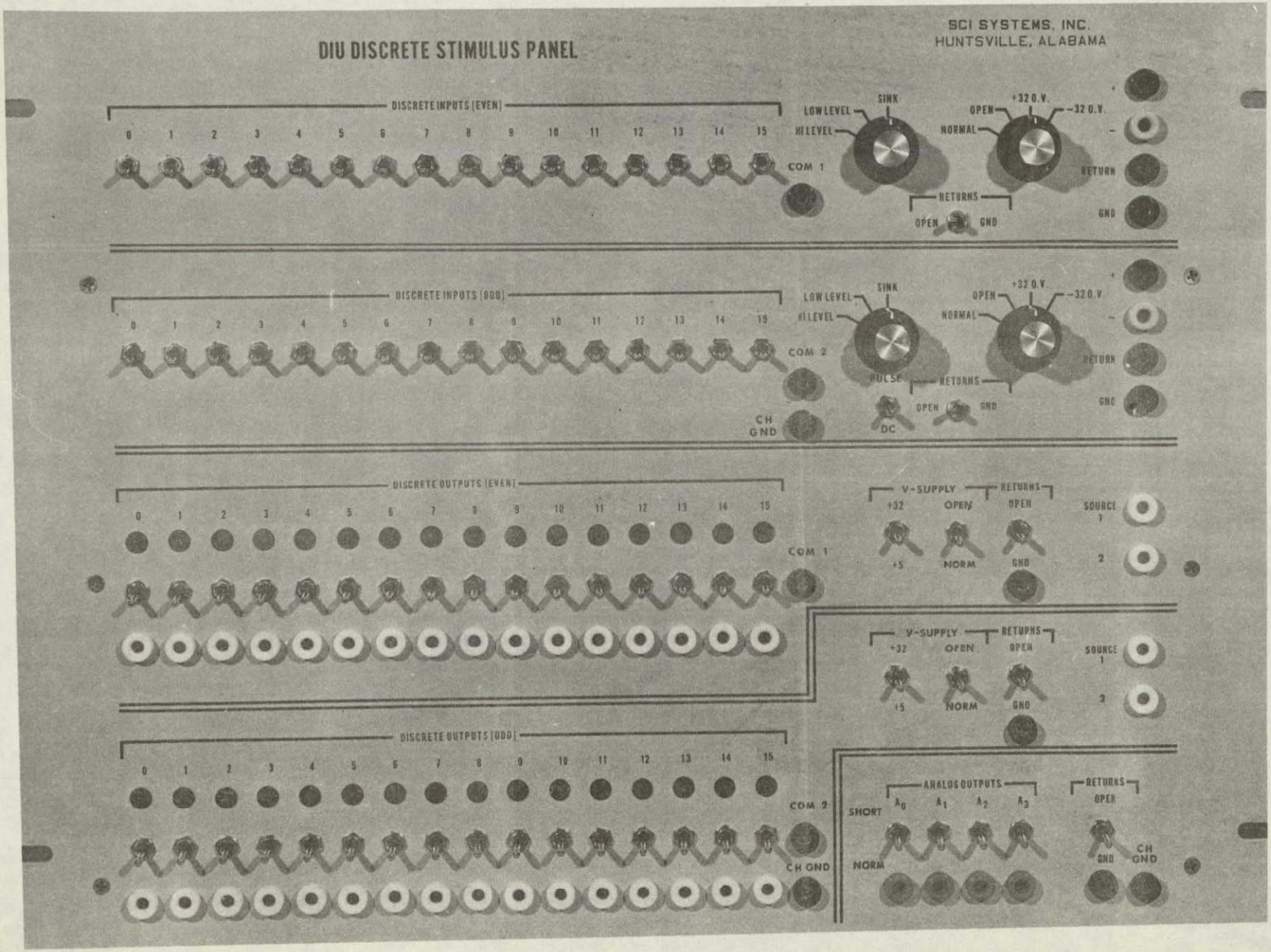


Figure 3.3-1

4.0 DIU TEST SYSTEM INTERNAL FUNCTIONAL DESCRIPTION

4.1 POWER SUPPLIES

Three power supplies are incorporated into each TCU, two 5 volt supplies, ± 15 volt supply and a 24-50 volt supply used to power the DIU under test. The second 5 volt supply was added due to the complexity of the test set and the requirements of the display LED's. Manufacturer specification sheets are provided in Figures 4.1-1, 4.1-2 and 4.1-3 as aids in troubleshooting, alignment and replacement of the units. The physical mounting location of the power supplies is on the under side of the circuit card chassis. All internal voltages are brought to a terminal block for distribution to the system, and external fusing of the supplies is provided. Figure 4.2-1 shows the locations of the fuses and distribution terminal block.

The Stimulus Panel has three power supplies for logic and limits testing in addition to the Precision Analog Source. The manufacturer's data sheets for the 32 volt supplies are shown in Figures 4.1-4 through 4.1-7.

POWERTEC
AN AIRTRONICS SUBSIDIARY
9168 DESOTO AVENUE
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(213) 882-0004 TWX 910-494-2092

APPLICATION DATA
OEM SERIES
TRIPLE OUTPUT
DC POWER SUPPLY

MODEL 2R-70T

SPECIFICATIONS

AC INPUT: 105 to 125VAC, 47 to 63Hz (Derate Unit 15% for 50Hz operation). For wider range or 400Hz operation, consult the factory.

DC OUTPUT RATINGS:

OUTPUT	OUTPUT (1) VOLTAGE	MAX. OUTPUT CURRENT	XFMR (2) TERMINALS
A1	12 V 15 V	1.5 A 1.3 A	12 V 15 V
A2	12 V 15 V	1.5 A 1.3 A	12 V 15 V
A3	5 V	6 A	N/A

(1). Adj. range ± 5%

(2). See outline drawing

REGULATION: Line ± 0.25%, Load ± 0.25%

OUTPUT RIPPLE: 1 mV RMS, 3 mV p to p

TRANSIENT RESPONSE: 50μ sec. for 50% load change.

OVERLOAD PROTECTION: Unit is protected from overload & short circuit using the current fold-back method.

INPUT FUSING: 2A input fusing is recommended for power supply protection.

COOLING: Convection cooled. Moving air is desirable when mounted in a confined area. Do not restrict airflow through baseplate for maximum ratings.

OPERATING TEMPERATURE: See table below

PERCENT OF FULL RATED LOAD AT AMBIENT TEMPERATURE			
+40°C	+50°C	+60°C	+71°C
100%	75%	50%	35%

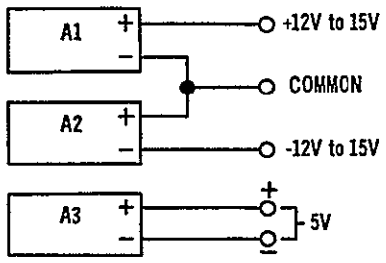
CONSTRUCTION: All aluminum, anodized

WEIGHT: 8.2 Pounds

CONNECTIONS FOR VARIOUS VOLTAGES

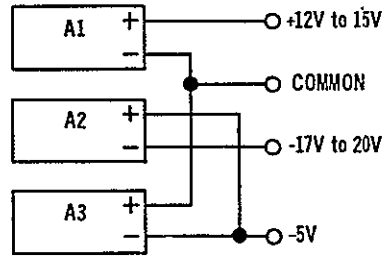
BASIC CONFIGURATION

OUTPUTS
A1) +12V to 15V
A2) -12V to 15V
A3) 5V floating



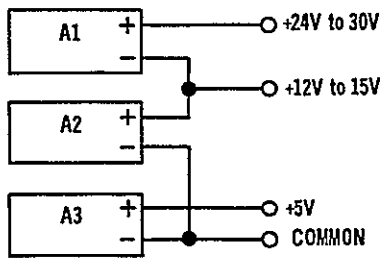
OPTIONAL

OUTPUTS
1) -5V
2) +12V to 15V
3) -17V to 20V



OPTIONAL

OUTPUTS
1) +24V to 30V
2) +12V to 15V
3) +5V



OPTIONAL

OUTPUTS
1) +17V to 20V
2) -12V to 15V
3) +5V

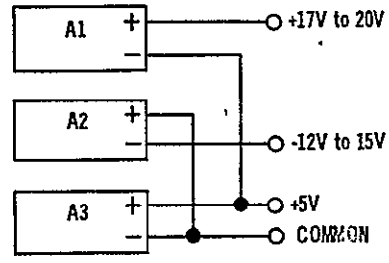
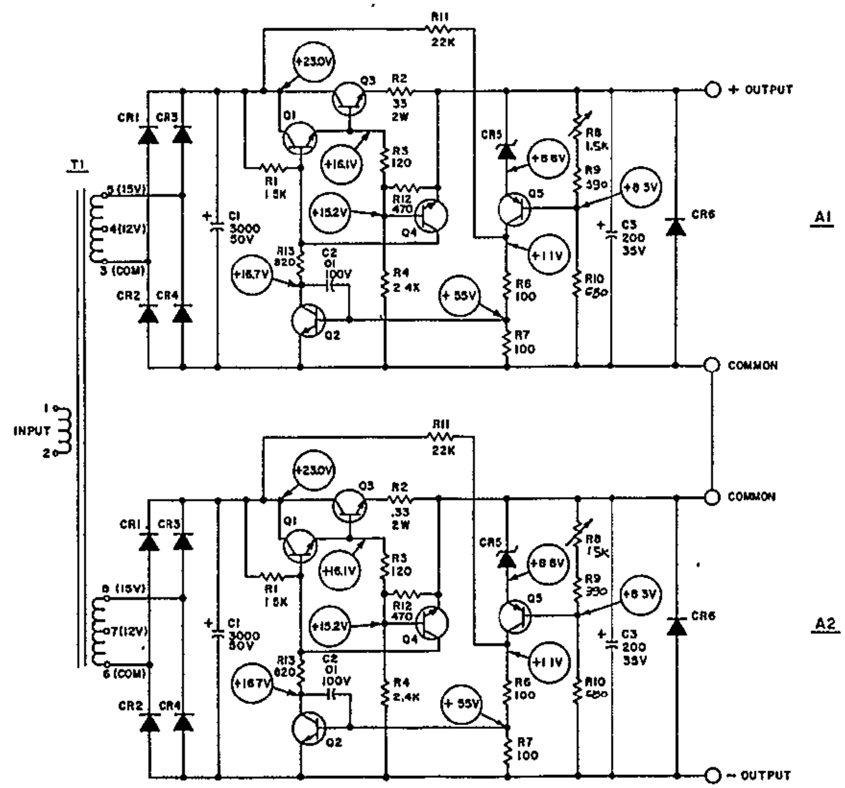


Figure 4.1-1 (a)

15092-002.

REV	DESCRIPTION	DATE	APPROVED
A	SEE ECN 011331	2-15-72	

REF DES (A1 & A2)	POWERTEC P/N	COM'L EQUIV	DESCRIPTION
C1	32-13007-012	STM39CS50AA33	3000 MFD, 50V
C2	31-13005-003	NPC-EL	.01 MFD, 100V
C3	32-13006-004	IEC-PCZ200FK35	200 MFD, 35V
CR1-4	11-13010-001	SEMTECH-351E	—
CR5	12-13013-008	1N4735A	—
CR6	11-13009-001	SEMTECH-S1-2	—
R1	20-13004-077	RC20GF152J	1.5K, 1/2W, 5%
R2	24-13014-007	IRC-BWH	.33Ω, 2W, 10%
R3	20-13004-051	RC20GF121J	120Ω, 1/2W, 5%
R4	20-13004-082	RC20GF242J	2.4K, 1/2W, 5%
R6,7	20-13004-049	RC20GF101J	100Ω, 1/2W, 5%
R8	23-13016-002	CTS-111	1500Ω
R9	20-13004-0[illegible]3	RC20GF391J	390Ω, 1/2W, 5%
R10	20-13004-069	RC20GF681J	680Ω, 1/2W, 5%
R11	20-13004-105	RC20GF223J	22K, 1/2W, 5%
R12	20-13004-065	RC20GF471J	470Ω, 1/2W, 5%
R13	20-13004-071	RC20GF821J	820Ω, 1/2W, 5%
Q1,2,4	10-13018-001	2N2219A	—
Q3	10-13002-003	2N3055	—
Q5	10-13021-001	2N2905A	—
A1,2	55-12795-001	—	PCB, 2B15V-24V
T1	40-13965-001	—	—



3. OPTION ON R8 23-13016-005 (CTS-XPC-110, 500Ω)
2. TEST VOLTAGES ARE TAKEN AT FULL RATED LOAD CURRENT, 115VAC INPUT. OUTPUT VOLTAGE ADJUSTED TO 15.0 VOLTS
1. TEST VOLTAGES ARE REFERENCED TO COMMON OUTPUT FOR + SUPPLY (A1)
TEST VOLTAGES ARE REFERENCED TO NEGATIVE OUTPUT FOR – SUPPLY (A2)

NOTE: UNLESS OTHERWISE SPECIFIED

LIST OF MATERIALS

CONTRACT NO.

APPD 7 22 71
CHECK 7/21/71
DRAWN 6-28-71

POWERTEC DIVISION
AIRTRONICS INCORPORATED
CHATSWORTH, CALIF.

TITLE: OEM SERIES 15D-13A

SIZE: D | CODE IDENT NO. 24429 | DRAWING NUMBER 13984 | REV B

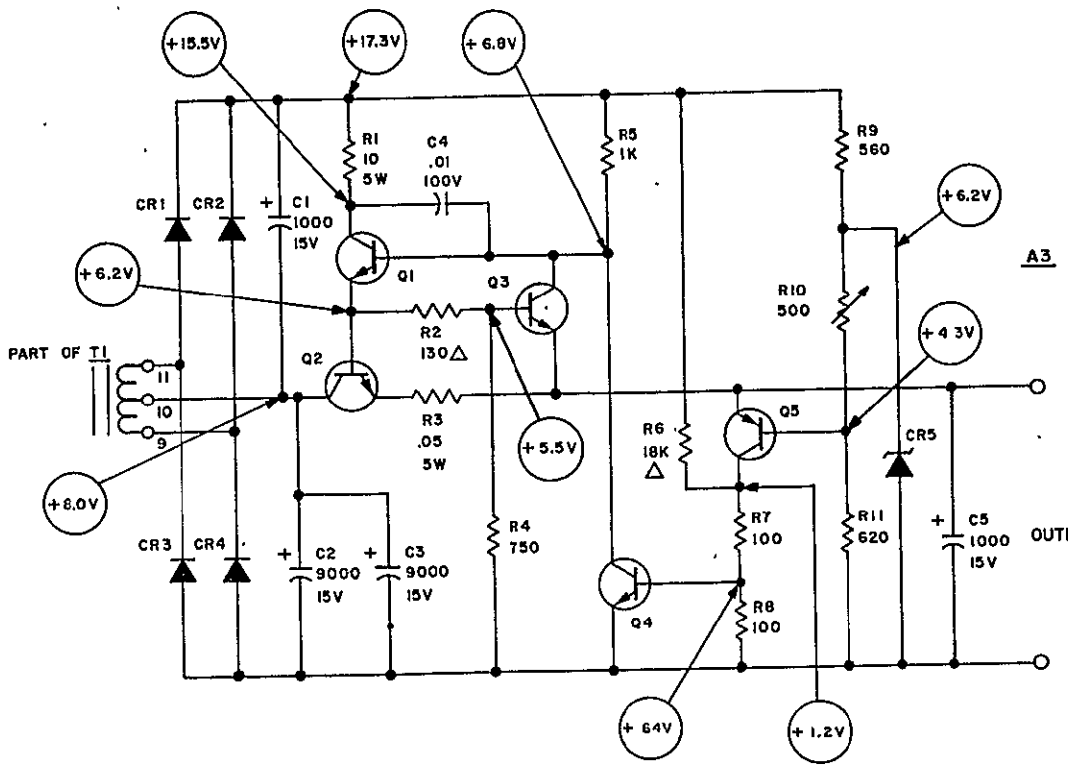
SCALE — | SHEET 1 OF 1

13984

Figure 4.1-1 (b)

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	SEE ECN 011037	10 6-71	
B	SEE ECN 011128	11-10-71	

SYM	POWERTEC P/N	COM'L EQUIV	DESC
C1,5	32-13006-003	PCZ1000PN15	1000 MFD, 15V
C2,3	32-13008-001	STM23C15AA93	9,000 MFD, 15V
C4	31-13005-003	NPC-EL	.01 MFD, 100V
CR1,2	11-13009-001	SI-2	—
CR3,4	11-13012-001	1N1200	—
CR5	12-13013-008	IN4735A	—
R1	22-13049-002	PW5-10Ω,10%	10Ω, 5W, 10%
R7,8	20-13004-049	RC20GF101J	100Ω, 1/2W, 5%
R3	22-13280-001	KS500	.05Ω, 5W, 5%
R4	20-13004-070	RC20GF751J	750Ω, 1/2W, 5%
R5	20-13004-073	RC20GF102J	1K, 1/2W, 5%
R6 △	20-13004-103	RC20GF183J	18K, 1/2W, 5%
R9	20-13004-067	RC20GF561J	560Ω, 1/2W, 5%
R10	23-13016-001	CTS-111	500Ω
R11	20-13004-068	RC20GF621J	620Ω, 1/2W, 5%
Q1,2	10-13002-003	2N3055	—
Q3,4	10-13018-001	2N2219A	—
Q5	10-13021-001	2N2905A	—
P.C.B.	55-12891-001	—	—
T1	40-13967-001	—	—
R2 △	20-13004-052	RC20GF131J	130Ω, 1/2W, 5%



COPY 15033 B

ORIGINAL PAGE IS OF POOR QUALITY

3. TEST VOLTAGES ARE TAKEN AT FULL RATED LOAD CURRENT, 115 VAC INPUT. OUTPUT VOLTAGE ADJUSTED TO 5.0 VOLTS.

2. ALL VOLTAGES ARE REFERENCED TO NEGATIVE OUTPUT.

1. △ INDICATES NOMINAL VALUE.

NOTE UNLESS OTHERWISE SPECIFIED

QTY REQD	PART NO OR TYPE DESIGNATION	SYM	NOMENCLATURE OR DESCRIPTION	CODE IDENT	MATERIAL NOTES AND SPECIFICATIONS	ITEM NO

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .060
ANGLES X° ± 1-0 XX ± .030
X°X' ± 0-30' XXX ± .010
DIM AND TOL PER MIL STD 8
MACHINED DIA S ON COMMON CENTER CONCENTRIC WITHIN .005 T I R
125 MACHINED SURFACE ROUGHNESS PER MIL STD 10
REMOVE BURRS BREAK EDGES .010 MAX
DO NOT SCALE DRAWING
REPORT ERRORS TO ENGINEERING DEPT
DO NOT MAKE CHANGES WITHOUT PROPER AUTHORIZATION

NEXT ASSY | FINAL ASSY
MATERIAL
FINISH

CONTRACT NO

APPD	Gilleise	7-22-71
CHECK		7/21-71
DRAWN	C LEEDY	7/7/71
APPROVED		
APPROVED		

POWERTEC DIVISION
AIRTRONICS INCORPORATED
9168 DESOTO AVE., CHATSWORTH CALIF 91311

TITLE
OEM SERIES
5V — 6A

SIZE	CODE IDENT NO	DRAWING NUMBER	REV
C	24429	15033	B

SCALE — SHEET 1 OF 1

Figure 4.1-1 (c)

TROUBLESHOOTING GUIDE

Check voltage test points shown on schematic 13984 for ease of failure determination.
(Applies to A1 or A2)

FAILURE INDICATION:	CHECK:
1. High input current, blows fuses.	C1 shorted
	CR1-CR4 shorted
2. Poor regulation, high output ripple.	C1 open
	CR1-CR4 open
	Q3 shorted
	possible output overload
3. High output voltage and ripple, poor regulation.	Q1, Q3 shorted
	Q2 open
4. Low output voltage with excessive ripple.	C3 leaky
	CR1-CR4 open
	Q4 shorted
	possible output overload
5. Excessive unit heating.	improper input frequency or voltage
	possible output overload
	inadequate ventilation
	improper transformer tap connection (See schematic)

Check voltage test points shown on schematic 15033 for ease of failure determination.
(Applies to A3)

FAILURE INDICATION:	CHECK:
1. High input current, blows fuses.	C1-C3 shorted
	CR1-CR4 shorted
2. Poor regulation, high output ripple.	C1-C3 open
	CR1-CR4 open
	Q2 shorted
	possible output overload
3. High output voltage and ripple, poor regulation.	Q1, Q2 shorted
	Q4 open
4. Low output voltage with excessive ripple.	C5 leaky
	CR1-CR4 open
	Q3 shorted
	possible output overload
5. Excessive unit heating.	improper input frequency or voltage
	possible output overload
	inadquate ventilation
	improper transformer tap connection (See schematic)

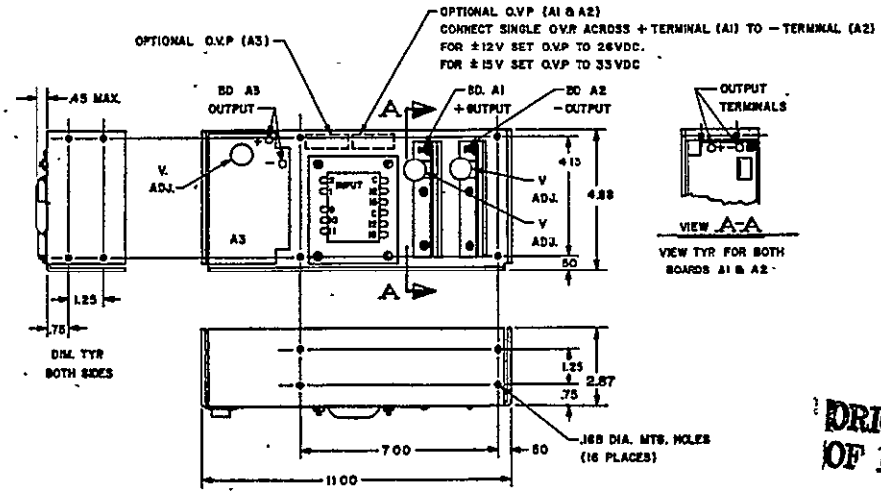


Figure 4.1-1 (d)

POWERTEC
AN AIRTRONICS SUBSIDIARY
9168 DESOTO AVENUE
CHATSWORTH CALIFORNIA 91311
(213) 882-0004 TWX 910-494-2092

APPLICATION DATA
CR SERIES DC POWER SUPPLY
MODELS 10B300
10C600

SPECIFICATIONS

AC INPUT: 105 to 125VAC, 47 to 63Hz

DC OUTPUT RATINGS: The CR series units are designed to be utilized at either 25 VDC or 50 VDC maximum output voltage by a simple reconnection of the transformer and filter circuits. Reduce maximum output current 15% for operation at 50Hz.

MODEL	25V CONNECTION		50V CONNECTION	
	E out	I out	E out	I out
10B300	12 - 25 VDC	12 Amps. Max.	24-50 VDC	6 Amps. Max.
10C600	12-25 VDC	24 Amps. Max.	24 - 50 VDC	12 Amps. Max.

REGULATION: Line ±1% + 50 mV Load ±1% + 50 mV

OUTPUT RIPPLE: 25V CONNECTION 300 mV RMS
50V CONNECTION 600 mV RMS

These ripple values may be reduced to 150 mV & 300 mV RMS respectively by addition of the optional ripple reducing kits.

OVERLOAD PROTECTION: Unit is protected against overload & short circuit by an input circuit breaker.

COOLING: Convection cooled. Moving air is desirable when mounted in a confined area. Do not restrict airflow through baseplate for maximum ratings.

OPERATING TEMPERATURE: See table below:

PERCENT OF FULL RATED LOAD AT TEMP.			
+ 40°C	+ 50°C	+ 60°C	+ 71°C
100%	75%	50%	35%

CONSTRUCTION: All aluminum, anodized

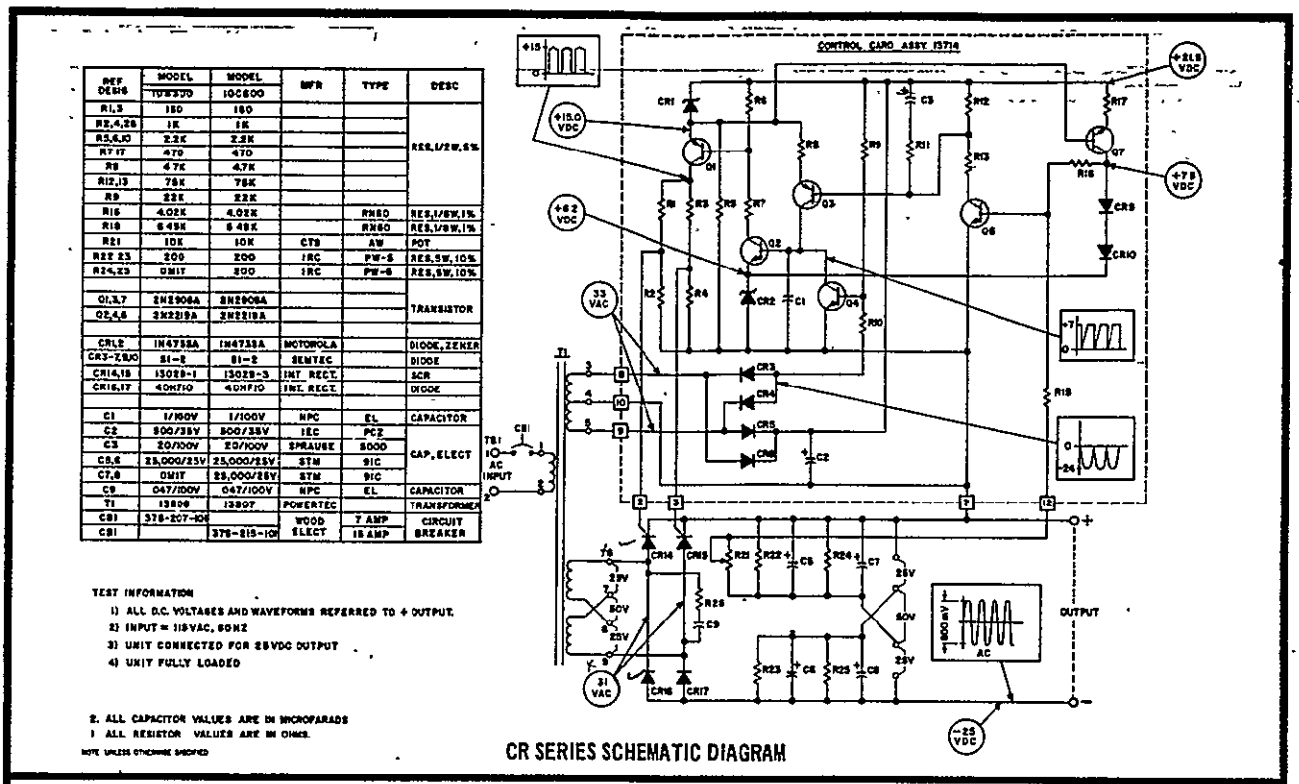
WEIGHT: MODEL 10B300 17 pounds
MODEL 10C600 32 pounds

TROUBLESHOOTING GUIDE

Check voltage test points shown on schematic for ease of failure determination.

FAILURE INDICATION:	CHECK:
1) High input current blows circuit breaker.	output overload or short
	C5-C8, CR14-CR17 or T1 shorted
	improper 25V/50V interconnection
2) High output voltage, no adjustment, no regulation	CR1, Q4, CR3, CR4, R21, C1, CR9, CR10 open
	Q1, Q2, Q3, Q6, CR1 Shorted
3) Low output voltage, no adjustment, no regulation	Q1, Q2, Q3, Q6, Q7, CR1, R1, R3, R16, R17 open
	Q4, CR9, CR10, R21, C1, CR3, CR4, shorted
4) High ripple or output oscillation	C5-C8, CR14-CR17, R11, C1, CR3, CR4 open
	if load is highly inductive or of a pulsed nature it may be necessary to adjust R11 and C3 for optimum stability.
5) Excessive unit heating	improper input voltage or frequency
	inadequate ventilation
	improper 25V/50V interconnection

Figure 4.1-2 (a)



REF DESIG	MODEL 10B300	MODEL 10C600	MFR	TYPE	DESC
R1,3	150	150			RES,1/2W,5%
R2,4,26	1K	1K			
R5,6,10	2.2K	2.2K			
R7 17	470	470			
R8	4.7K	4.7K			
R12,13	75K	75K			
R9	22K	22K			
R16	4.02K	4.02K		RN60	RES,1/8W,1%
R18	6.49K	6.49K		RN60	RES,1/8W,1%
R21	10K	10K	CTS	AW	POT
R22 23	200	200	IRC	PW-5	RES,5W,10%
R24,29	OMIT	200	IRC	PW-5	RES,5W,10%
Q1,3,7	2N2906A	2N2904A			TRANSISTOR
Q2,4,6	2N2219A	2N2218A			
CR1,2	IN4738A	IN4738A	MOTOROLA		DIODE,ZENER
CR3-7,9,10	S1-2	S1-2	SEMTEC		DIODE
CR14,15	13028-1	13028-3	INT RECT		SCR
CR16,17	40HF10	40HF10	INT RECT		DIODE
C1	1/100V	1/100V	NPC	EL	CAPACITOR
C2	500/35V	500/35V	IEC	PC2	CAP,ELECT
C3	20/100V	20/100V	SPRAGUE	5000	
C5,6	25,000/25V	25,000/25V	STM	91C	
C7,8	OMIT	25,000/25V	STM	91C	
C9	.047/100V	.047/100V	NPC	EL	CAPACITOR
T1	13809	13807	POWERTEC		TRANSFORMER
CB1	378-207-106		WOOD ELECT	7 AMP	CIRCUIT BREAKER
CB1		378-215-109		15 AMP	

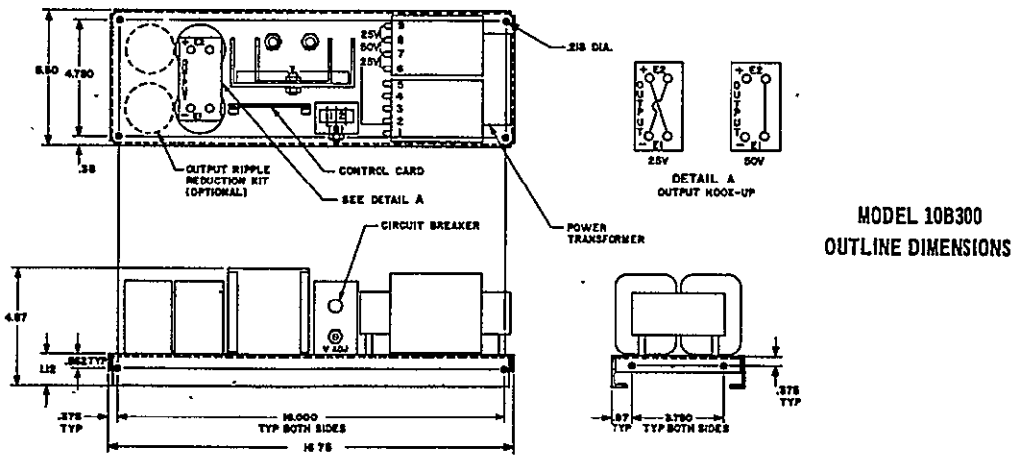
TEST INFORMATION

1) ALL D.C. VOLTAGES AND WAVEFORMS REFERRED TO + OUTPUT.
2) INPUT = 115 VAC, 60HZ
3) UNIT CONNECTED FOR 25 VDC OUTPUT
4) UNIT FULLY LOADED

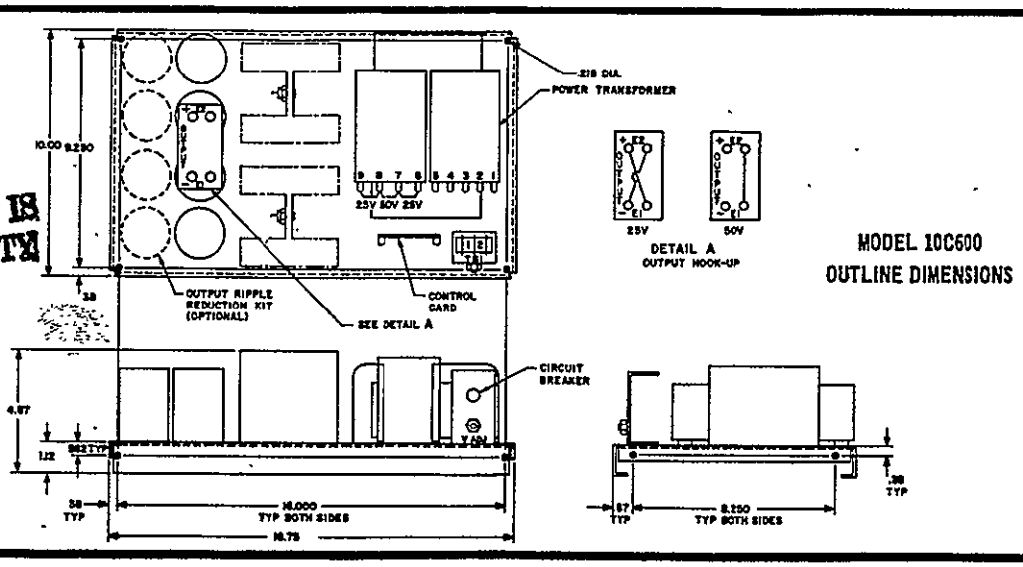
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
1 ALL RESISTOR VALUES ARE IN OHMS.

NOTE UNLESS OTHERWISE SPECIFIED

CR SERIES SCHEMATIC DIAGRAM



MODEL 10B300
OUTLINE DIMENSIONS



MODEL 10C600
OUTLINE DIMENSIONS

Figure 4.1-2 (b)

OEM SERIES
POWER SUPPLY MODULES

INSTRUCTION MANUAL

acdc electronics inc.

OCEANSIDE, CALIFORNIA

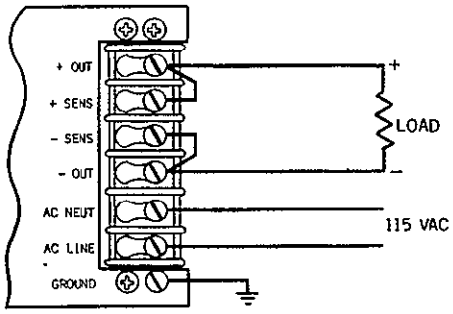
Figure 4.1-4

INPUT:	105-125 VAC, 47-63 Hz (Useable also at 400 Hz; consult factory for derating.)
OUTPUT:	Voltage is adjustable between limits by externally accessible screwdriver adjustment of a potentiometer. Output is floating; either positive or negative terminal may be grounded. Current: Zero to full load. Adjustment range: 4-8 Volt Models ± .25V 10-18 Volt Models ± .5V 20-32 Volt Models ± 1V Note: Voltage and current are coded by model no. Example: OEM5N5.7 is a 5 volt supply with a maximum current rating of 5.7 amp at 40°C.
REGULATION:	0.1% + 5 mV NL-FL, ±0.1% ±5 mV for 10% input change.
RIPPLE:	2 mV RMS max., 20 mV P-P max.
STABILITY:	Typically 10 mV for eight hour period after initial warmup.
TEMPERATURE COEFFICIENT:	0.02% / °C max.
OUTPUT IMPEDANCE:	DC-1KHz: 0.001 R_L or 0.005 ohm max. 1KHz-100KHz: 0.005 R_L or 0.5 ohm max. (R_L is the rated load)
TRANSIENT RESPONSE:	Output voltage returns to within regulation limits within 50 µsec in response to a 50% load step.
REMOTE SENSING:	Terminals are provided to maintain regulation at the load, compensating for the DC voltage drop in the load cable.
REMOTE VOLTAGE ADJUSTMENT:	Output voltage may be remotely adjusted over a limited range by insertion of a variable resistor in the positive sensing line.
OVERLOAD PROTECTION:	Inherently protected against overload and short circuit by a foldback type characteristic.
OVERVOLTAGE PROTECTION (OPTIONAL):	Any model can be furnished with overvoltage protection which crowbars the output in the event of a rise in the output voltage of between 1 to 2 volts or 10-20% (whichever is larger). This protection circuit is completely independent of the supply. The addition of overvoltage protection does not add to the outline dimensions of the supply. On dual models, overvoltage protection "crowbars" both voltages to near zero in the event of a rise of one or both of the voltages of 20% or 4 volts (whichever is greater).
AMBIENT TEMPERATURE:	Operating; 0 to 71°C. Storage: -50 to 85°C

SPECIFICATIONS - OEM SERIES

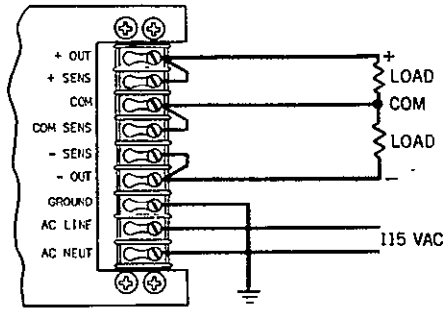
acdc electronics inc.

Figure 4.1-5



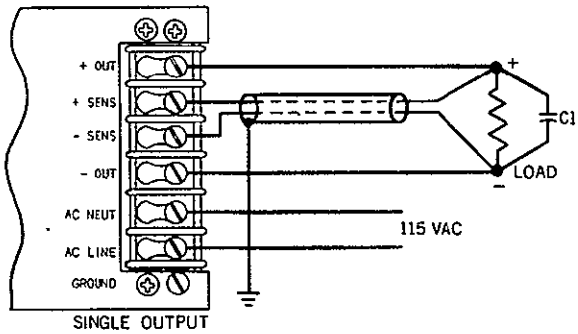
SINGLE OUTPUT, LOCAL SENSE

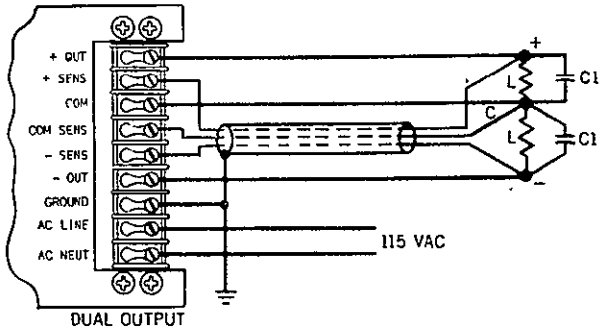
THE POSITIVE OR NEGATIVE OUTPUT MAY BE GROUNDED. A VOLTAGE ADJUSTMENT POTENTIOMETER IS ACCESSIBLE THROUGH A HOLE IN THE CASE. REGULATION SHOULD BE MEASURED AT THE BARRIER STRIP. THE POWER SUPPLY IS EQUIPPED WITH AUTOMATIC OVERLOAD PROTECTION



DUAL OUTPUT, LOCAL SENSE

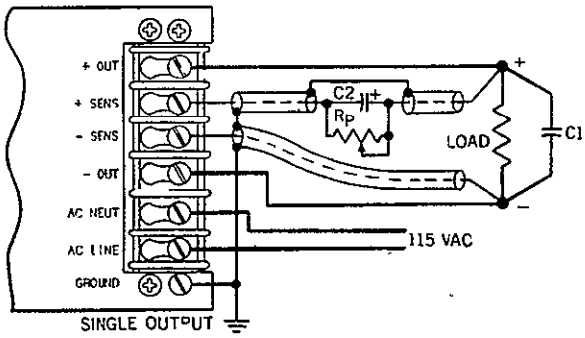
THE POSITIVE AND NEGATIVE OUTPUTS ARE REFFRENCED TO THE COMMON. THE OUTPUTS MAY BE ADJUSTED BY POTENTIOMETERS ACCESSIBLE THROUGH HOLES IN THE COVER. THE POWER SUPPLY IS EQUIPPED WITH AUTOMATIC OVERLOAD PROTECTION. THE POSITIVE OUTPUT IS THE MASTER. WHEN THE POSITIVE OUTPUT IS SHORTED BOTH OUTPUTS WILL BE TURNED OFF

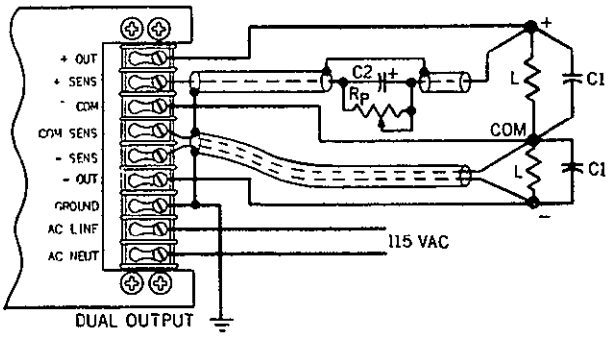




REMOTE SENSE

USE SHIELDED SENSE LEADS AND ROUTE FOR MINIMUM PICKUP. RUN POWER LEADS CLOSE TO EACH OTHER. A CAPACITOR (C1) IS SUGGESTED TO REDUCE THE OUTPUT IMPEDANCE AND IMPROVE CIRCUIT STABILITY. CAPACITOR VALUE SHOULD BE APPROXIMATELY 100MFD/AMP.





REMOTE VOLTAGE ADJUSTMENT

OBSERVE ALL INSTRUCTIONS FOR REMOTE SENSING. TO PROGRAM OUTPUTS, ADJUST VOLTAGE ADJUSTMENT POTENTIOMETERS FOR MINIMUM DC OUTPUT. CONNECT THE PROGRAMMING RESISTANCE (Rp) AS SPECIFIED, USING EXTREME CARE THAT LEADS ARE PERMANENTLY CONNECTED. DO NOT SWITCH. DO NOT ATTEMPT TO PROGRAM ABOVE OR BELOW SPECIFIED ADJUSTMENT RANGE. THE VALUE OF Rp SHOULD BE APPROXIMATELY 2000 OHMS PER VOLT. Rp MUST BE A LOW NOISE, TC TYPE RESISTOR. SHIELDED LEADS AND A CAPACITOR (C2) ARE NECESSARY TO MAINTAIN LOW RIPPLE. THE CAPACITOR SHOULD HAVE LOW LEAKAGE AND ESR.

GENERAL NOTES

THE OVERLOAD AND OVERVOLTAGE ADJUSTMENTS ARE CONSIDERED FACTORY ADJUSTMENTS. DO NOT MAKE ANY ADJUSTMENT WITHOUT CONSULTING FACTORY.

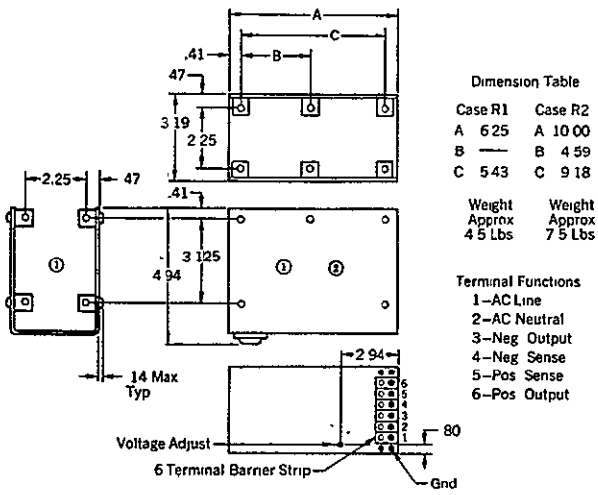
IF OVERVOLTAGE PROTECTION IS INCLUDED A LINE FUSE SHOULD BE INSTALLED BY THE USER FOR PROTECTION AGAINST CATASTROPHIC FAILURE

COMMON APPLICATION PROBLEMS

NO OUTPUT	NO AC INPUT, DEFECTIVE LINE FUSE, OUTPUT SHORTED, INCORRECT HOOK UP.
LOW OUTPUT	EXCESSIVE LOAD CURRENT, OVERVOLTAGE OPERATING, OUTPUT VOLTAGE ADJUSTED TOO HIGH, OPEN SENSE LEADS OR PROGRAMMING RESISTANCE.
HIGH OUTPUT	OPEN SENSE LEADS.

TO RECYCLE OVERVOLTAGE PROTECTION, THE AC INPUT MUST BE REMOVED FOR APPROXIMATELY 2 SECONDS AND THEN REAPPLIED.

Case R1 & R2

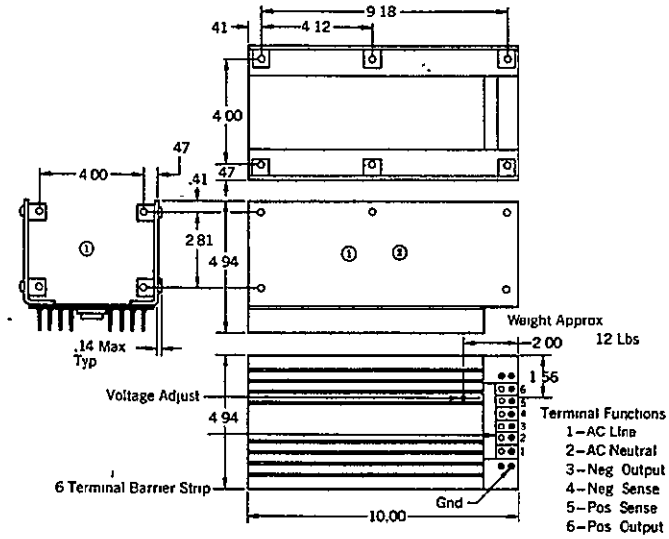


Dimension Table

Case R1		Case R2	
A	6 25	A	10 00
B	—	B	4 59
C	5 43	C	9 18
Weight Approx	4 5 Lbs	Weight Approx	7 5 Lbs

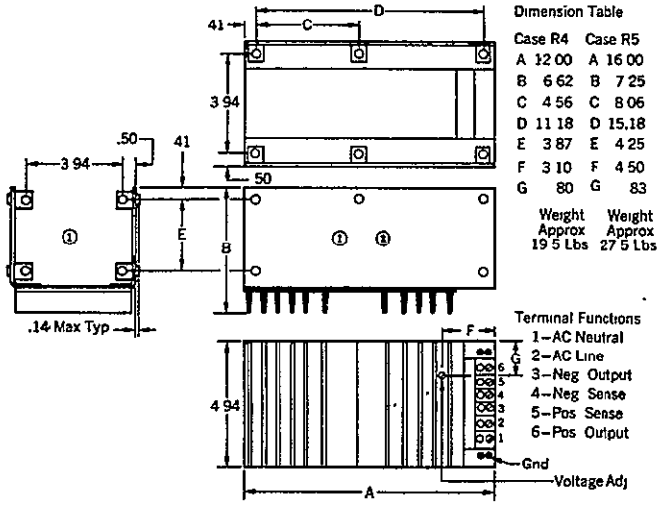
Terminal Functions
1–AC Line
2–AC Neutral
3–Neg Output
4–Neg Sense
5–Pos Sense
6–Pos Output

Case R3



Terminal Functions
1–AC Line
2–AC Neutral
3–Neg Output
4–Neg Sense
5–Pos Sense
6–Pos Output

Case R4 & R5

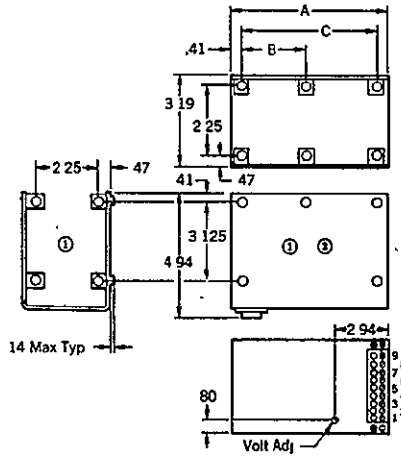


Dimension Table

Case R4		Case R5	
A	12 00	A	16 00
B	6 62	B	7 25
C	4 56	C	8 06
D	11 18	D	15.18
E	3 87	E	4 25
F	3 10	F	4 50
G	80	G	83
Weight Approx	19 5 Lbs	Weight Approx	27 5 Lbs

Terminal Functions
1–AC Neutral
2–AC Line
3–Neg Output
4–Neg Sense
5–Pos Sense
6–Pos Output

Dual Modules R1 & R2



Dimension Table

Case R1		Case R2	
A	6 25	A	10 00
B	—	B	4 59
C	5 43	C	9 18
Weight Approx	4 5 Lbs	Weight Approx	7 5 Lbs

Terminal Functions
1–AC Neutral
2–AC Line
3–Gnd
4–Neg Output
5–Neg Sense
6–Common Sense
7–Common
8–Pos Sense
9–Pos Output

① This mounting pattern is repeated on opposite side for a total of 5 possible mounting faces.
Note: All mounting holes have threads to receive #8Z screws.

② Provide clearance holes as required for screwheads on this surface.

OUTLINE AND MOUNTING DIMENSIONS--OEM SERIES
acdc electronics

Figure 4.1-7

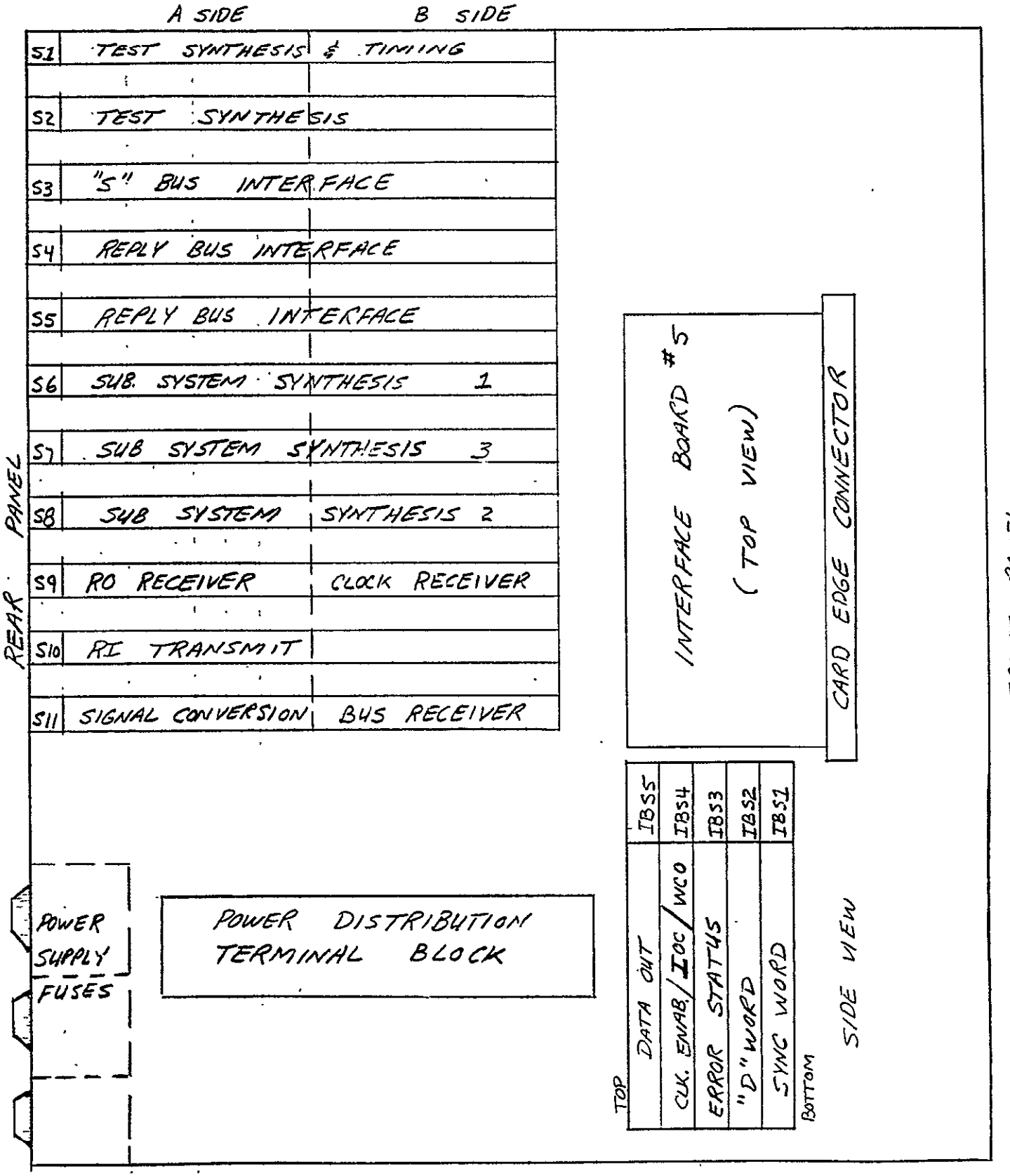
4.2 MECHANICAL OUTLINE

The circuits are layed out on wired printed circuit boards with distribution via card edge connectors and point to point chassis wiring. Figure 4.2-1 shows the chassis layout for the TCU circuit boards, fuses,and power distribution terminal block. Rear panel connectors have been deleted since they mirror those of the DIU under test. The front panel layout is shown in Figure 2.1-1 and its operation is described in Section 2.

Cooling air to the TCU is provided by three muffin type fans pushing air past the internal circuits with all of the panels in place. It is important to ensure the unit is operated with the sides and top in place to avoid overheating of components.

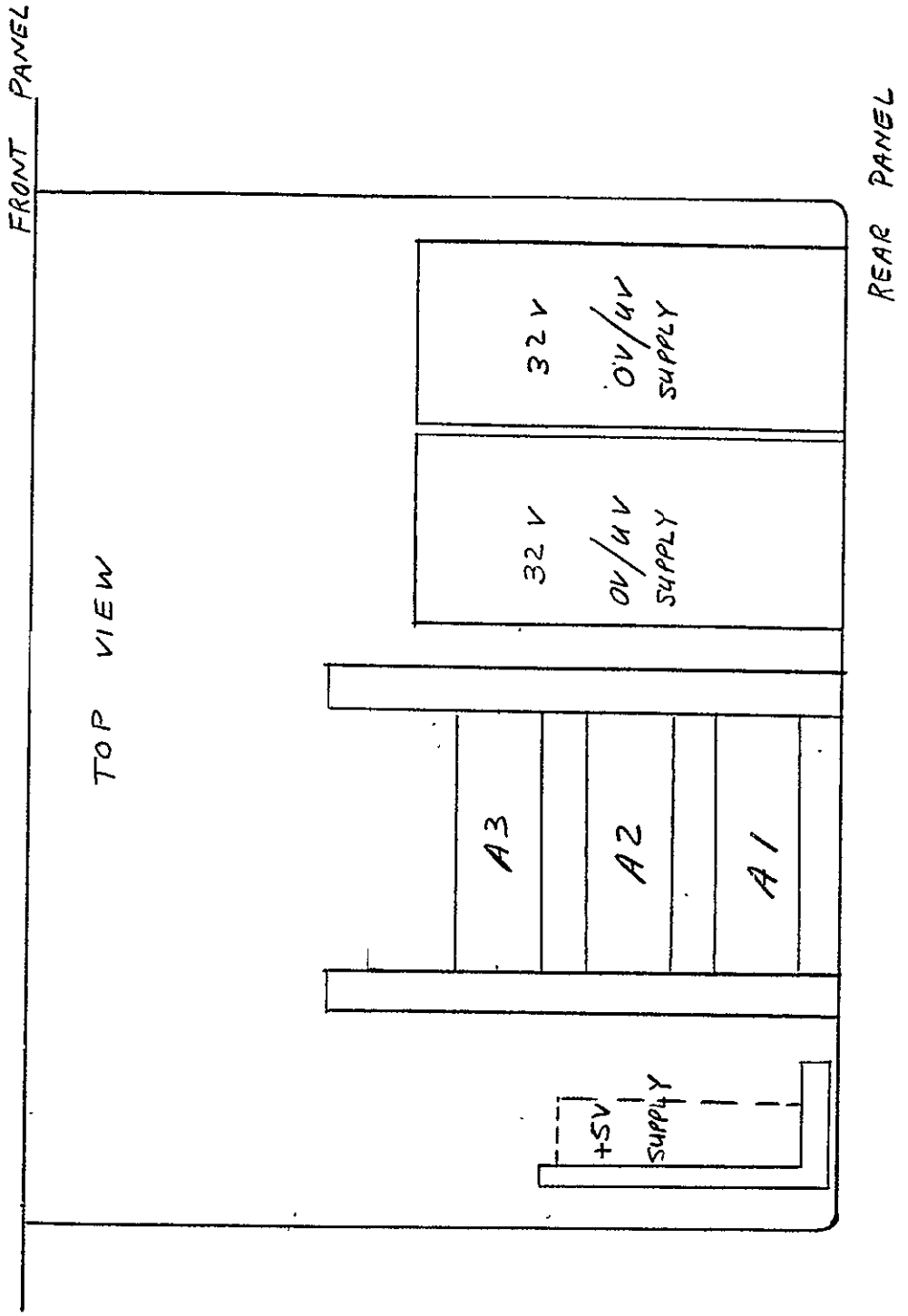
The stimulus panel consists mainly of load resistors, power sources, control switches and indicator LED's. It is an open frame structure and any fault isolation can be done with the aid of the schematics shown in Appendix A since they follow a flow chart arrangement. This is due to the basic switch logic implementation.

For the DI's and DO's three circuit boards are utilized for loads and lamp drivers. Figure 4.2-2 shows the arrangement of these cards behind the Discrete Stimulus Panel and the placement of the power sources. Reference is made to DWG 3339550, in Appendix A, for components located on each card. Figures 4.2-3 and 4.2-4 show the rear panel layouts for the Discrete and Analog Stimulus Panels respectively.



TCU MECHANICAL OUTLINE

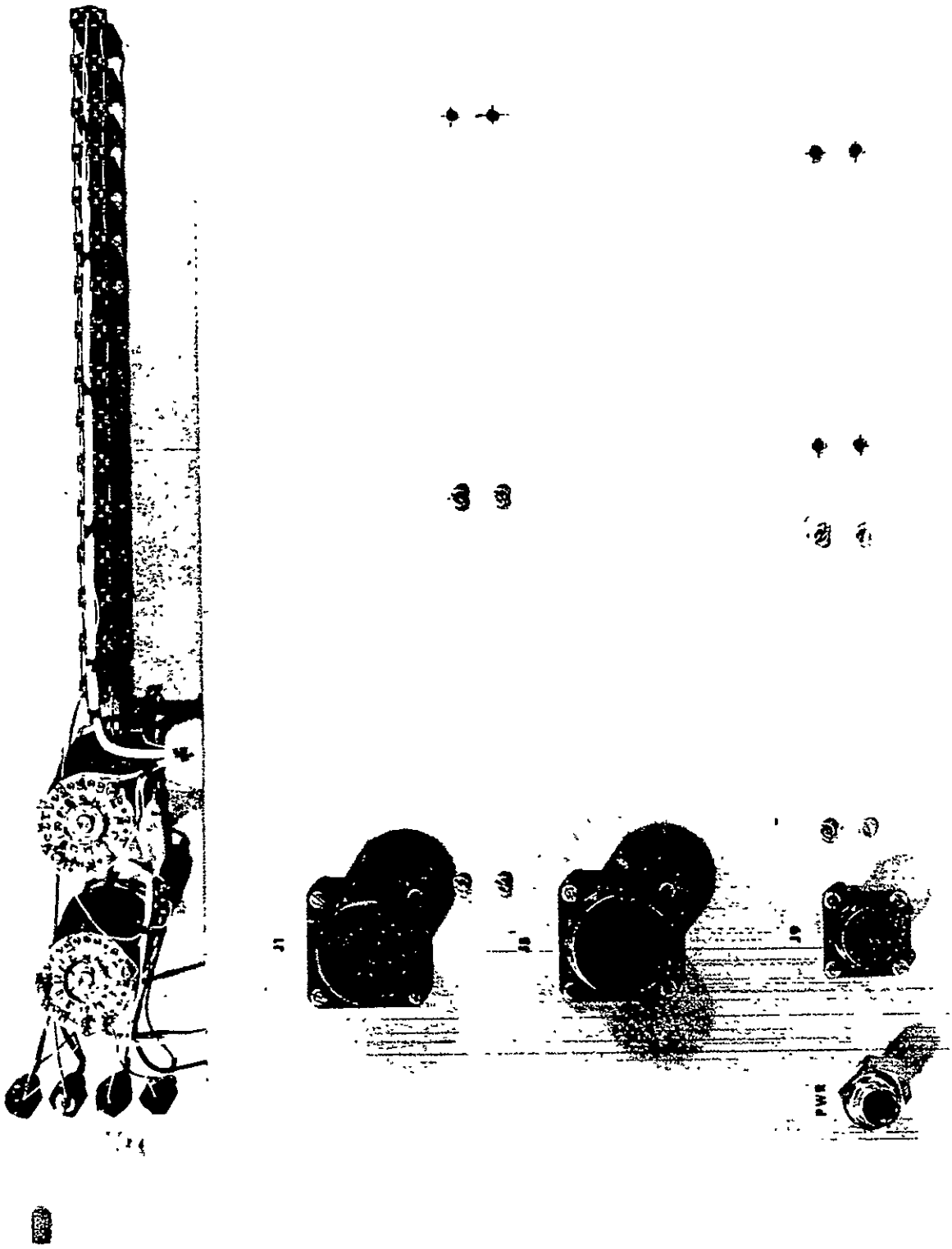
Figure 4.2-1



REF. DWG.
3339 550

DISCRETE STIMULUS. PANEL OUTLINE.

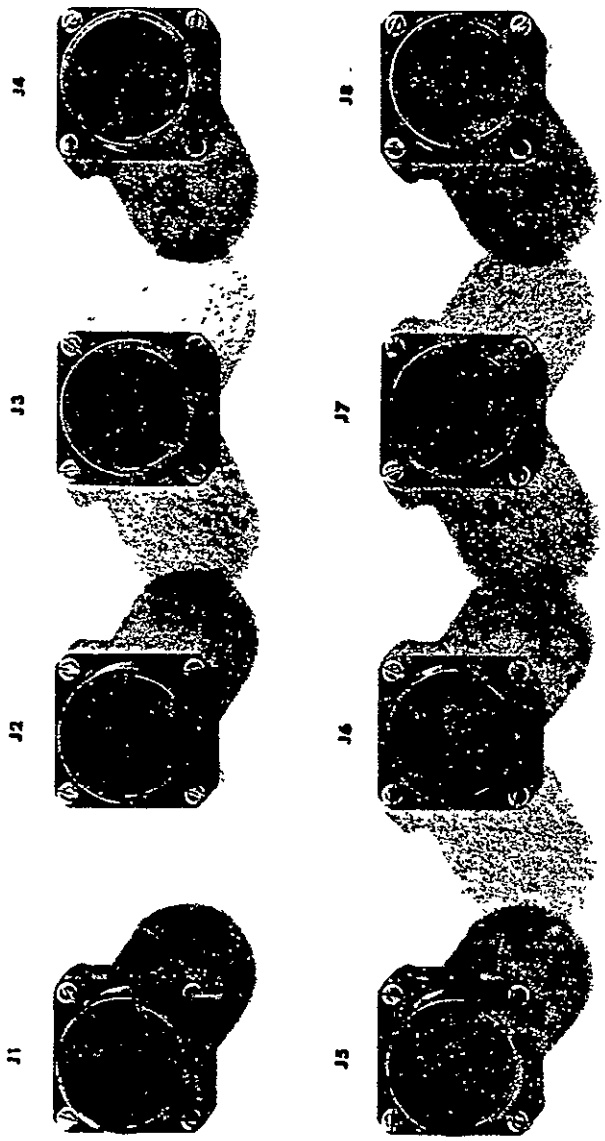
Figure 4.2-2



DISCRETE STIMULUS PANEL

REAR VIEW

Figure 4.2-3



ANALOG STIMULUS PANEL
REAR VIEW
Figure 4.2-4

4.3 TCU/STP CIRCUIT BLOCK DIAGRAM DESCRIPTIONS

4.3.1 Introduction

The block diagram circuit descriptions will be presented by examining the system functionally at the P.C. board level. Therefore, each block diagram corresponds to a single card starting with card S1, Figure 4.3-1, and proceeding sequentially through card S11, Figure 4.3-15. Figure 4.3-16 is a block diagram which depicts the operation of the Stimulus Panel. Each section and diagram identifies which drawings in Appendix A are to be used in conjunction with the block diagrams for troubleshooting the system.

Using the information contained in the four sections of this report plus the schematics in Appendix A, repairs and modifications to the Test System can be accomplished with a minimum amount of difficulty by qualified personnel.

4.3.2 Board S-1 - Test Synthesis and Timing (3339510-1, 2)

The basic timing functions for the Supervisory Bus Interface portion of the TCU are generated on this card whose block diagram is shown in Figure 4.3-1. Since the Sub System (RI/RO) and the Reply Bus Interface sections are dependent on DIU transmitted data, their basic timing differs from that presented in this section, and will be covered later.

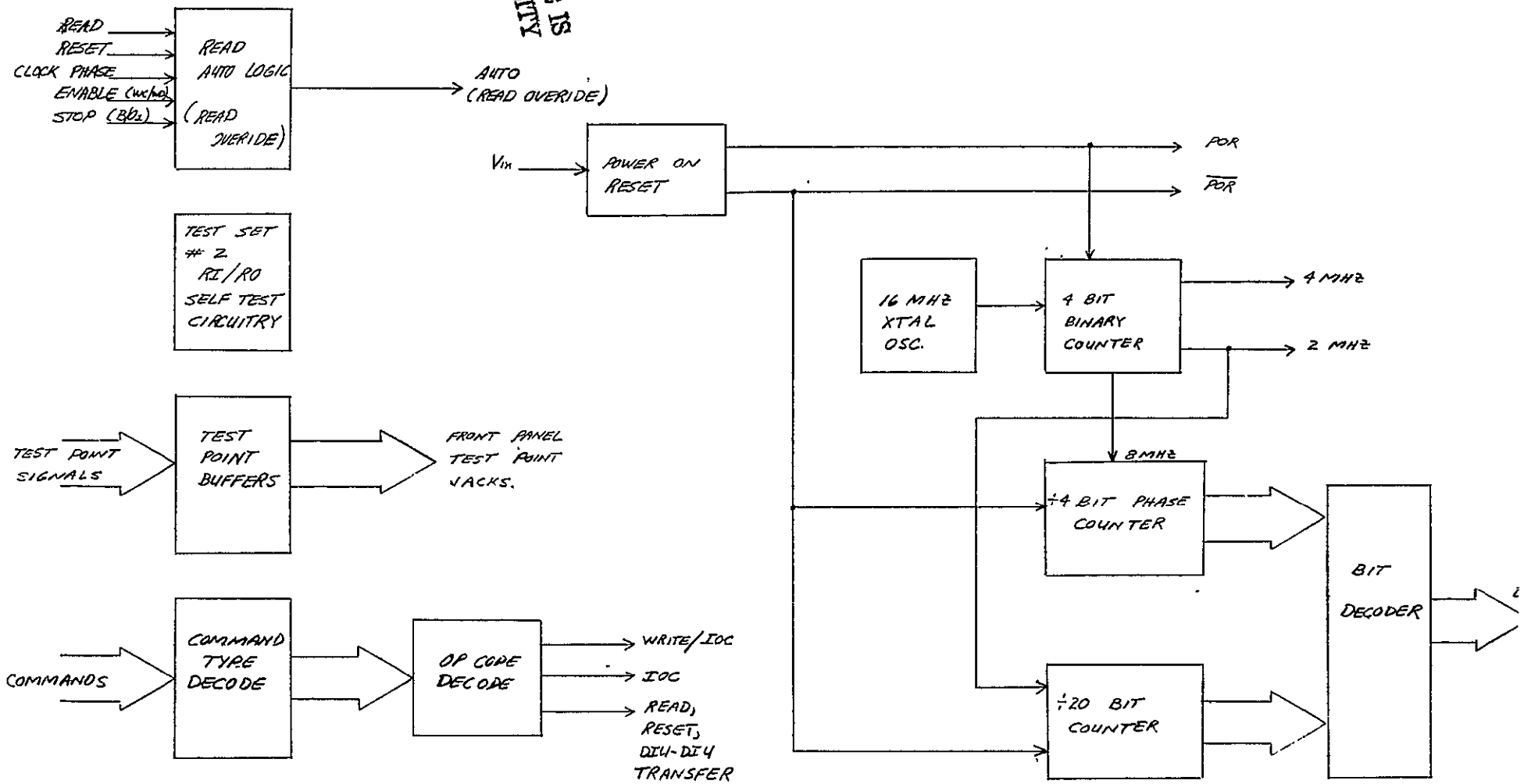
The three basic clocks derived from the 16 MHz crystal oscillator are 8 MHz, 4 MHz and 2 MHz system clocks. The 8 MHz clock is divided into clock phase bits by the ÷ 4 bit phase Johnson Counter. Each of the 4 phases generated is one fourth the 2 MHz bit time or 125 nano seconds wide (4 MHz rate). To avoid glitches when decoding only 3 of the 4 phases are actually used, these being ØW, ØX, and ØY. Figure 4.3-2 shows the basic bit phase timing and the bit phase decodes. The 2 MHz output clocks the ÷ 20 bit Johnson

Counter which generates the 20 bits necessary for system word timing. Each bit decoded is 500 nano-seconds wide and a total word time is then 500 x 20, or 10000, nano-seconds in duration. Figure 4.3-3 shows the bit counter timing and decodes. When the bits and bit phases are mixed in the decoder any combination of bit times and bit phase times can be obtained. An example would be a parity x phase pulse obtained from the parity bit decode and the x phase decode.

The TCU's power on reset pulse is also generated on this card, and is derived from a delayed signal being presented to a one-shot when power is initially applied. The RC time constant allows the one-shot to stabilize prior to the input triggering the reset pulse. A low impedance turn off path is used to discharge the capacitor latch and allow rapid recycling of the system power. The outputs from the one-shot are buffered on each card to prevent excessive loading on the reset circuitry.

Command type decoding is block decoded from switch inputs to allow for op code groupings as shown in Figure 4.3-1. The read and write commands plus an illegal op code flag are then decoded. Additionally, illegal op codes are combined with the write command, to verify proper DIU Rejection of this code. Therefore, the TCU executes an IOC command as if it were a write command.

Front panel test point buffer and a read override (read Auto) function complete the signals generated. The read auto function is explained in Section 2.2.4.2. The inputs to the Read Auto Logic start and stop the count during a read operation. This circuitry serves the same function as a "D" word enable during a write operation, that is, counting the number of words being transmitted on the Supervisory Bus.

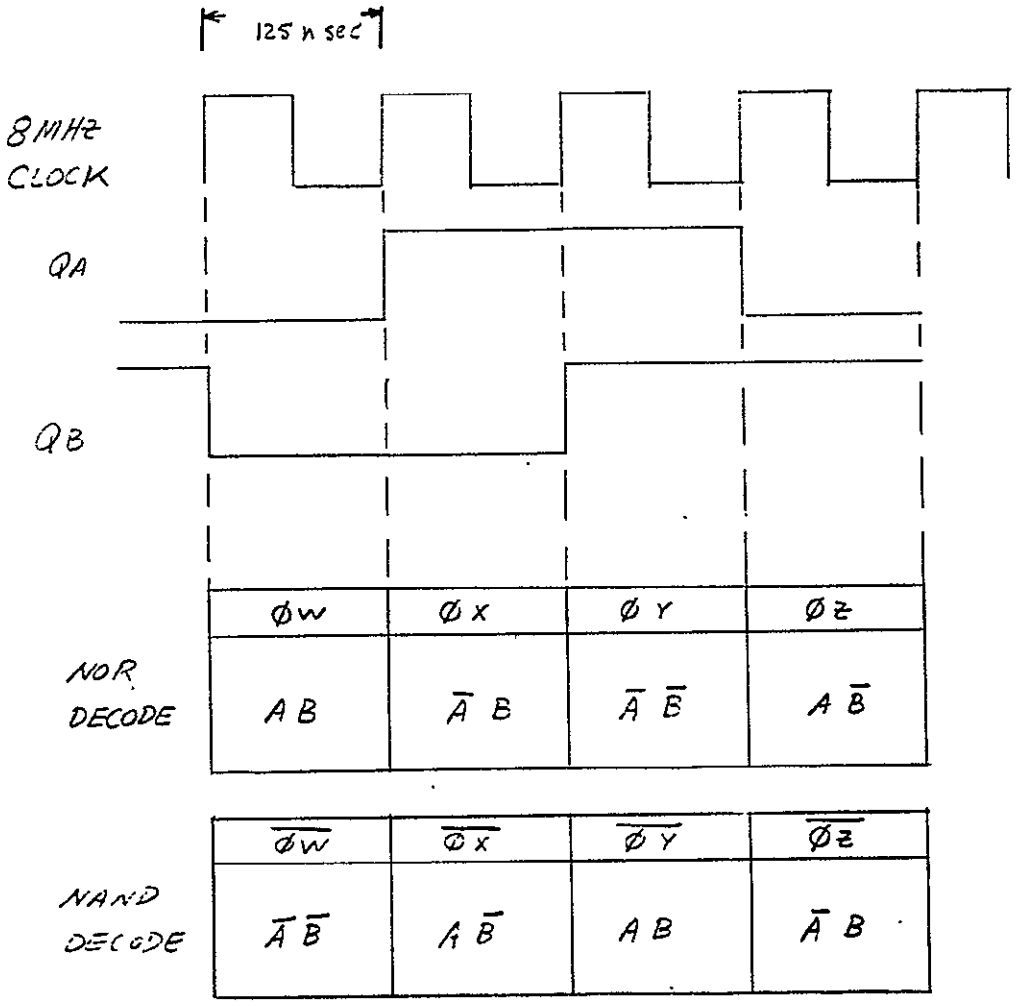


TEST SYNTHESIS TIMING

Figure 4.3-1

REF.
3339510-1
3339510-2

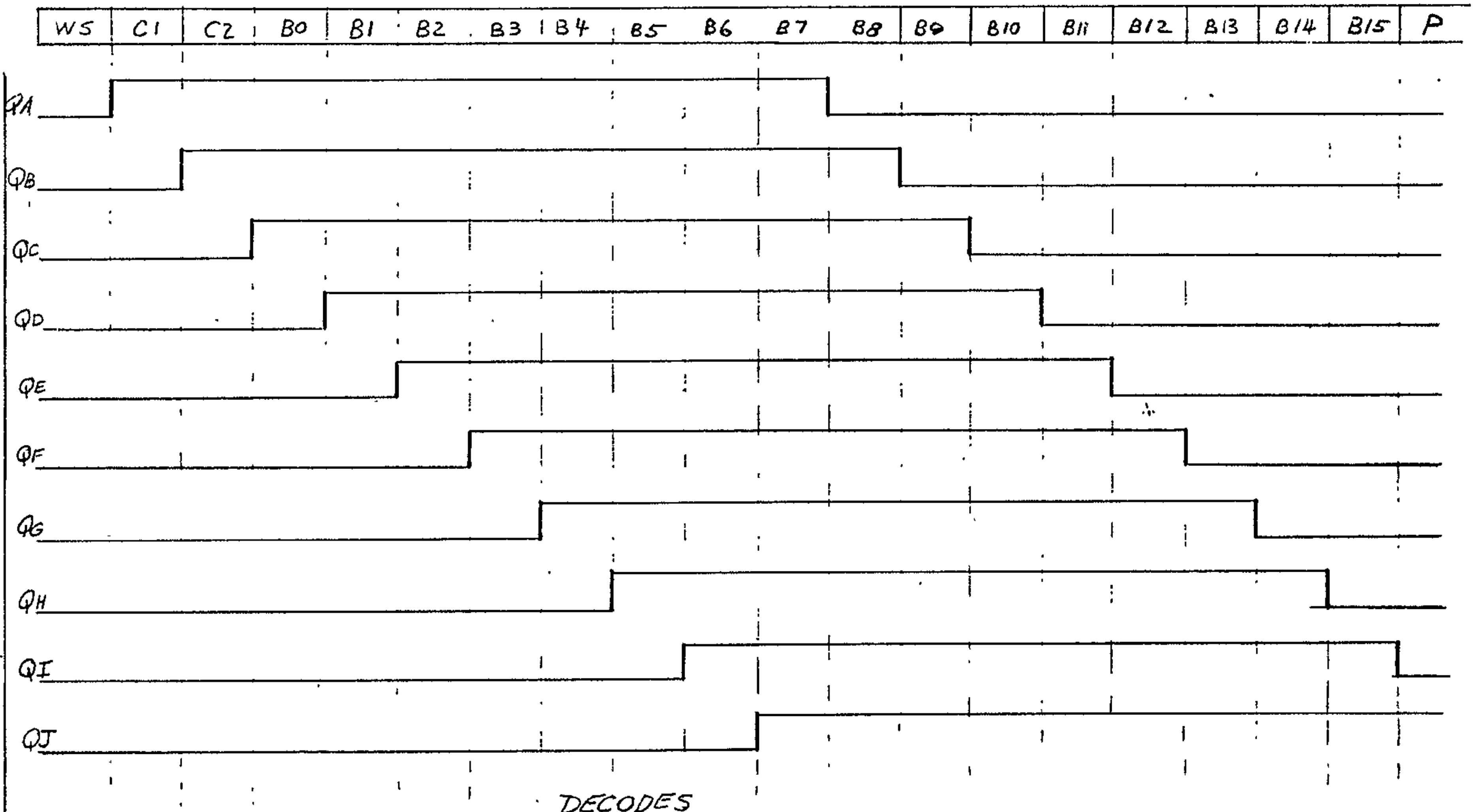
1-21-



BOARD S1 (3339510-1, 2)
÷4 JOHNSON COUNTER AND
BIT PHASE DECODES

FIGURE 4.3-2

FIGURE 4.3-3 (BOARD S1) 120 JOHNSON COUNTER & BIT DECODES



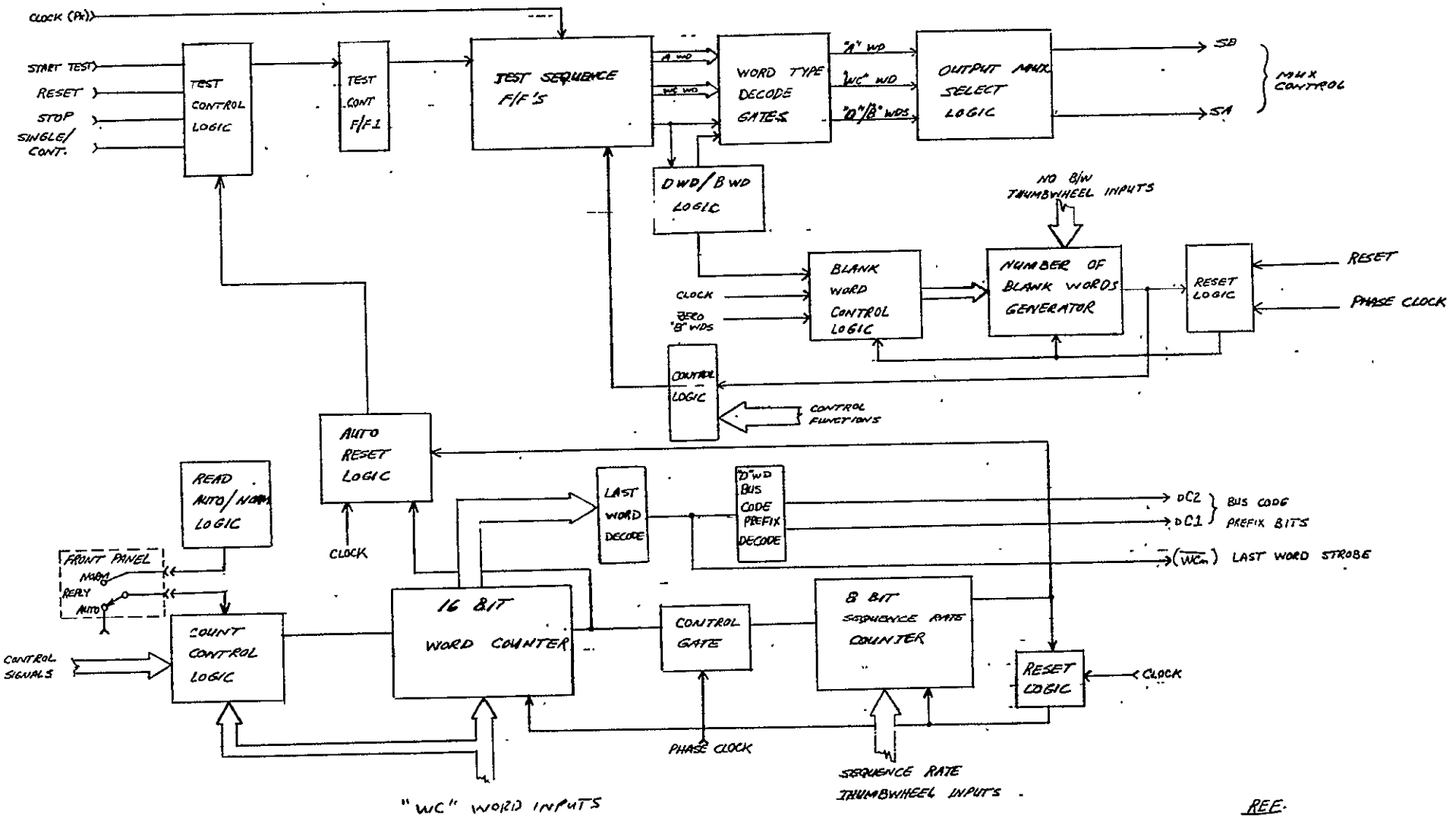
	WS	C1	C2	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	P
NOR DECODE	AJ	$\bar{A}B$	$\bar{B}C$	$\bar{C}D$	$\bar{D}E$	$\bar{E}F$	$\bar{F}G$	$\bar{G}H$	$\bar{H}I$	$\bar{I}J$	$\bar{A}\bar{J}$	$A\bar{B}$	$B\bar{C}$	$C\bar{D}$	$D\bar{E}$	$E\bar{F}$	$F\bar{G}$	$G\bar{H}$	$H\bar{I}$	$I\bar{J}$
NAND DECODE	$\overline{WS}$	$\overline{C1}$	$\overline{C2}$	$\overline{B0}$	$\overline{B1}$	$\overline{B2}$	$\overline{B3}$	$\overline{B4}$	$\overline{B5}$	$\overline{B6}$	$\overline{B7}$	$\overline{B8}$	$\overline{B9}$	$\overline{B10}$	$\overline{B11}$	$\overline{B12}$	$\overline{B13}$	$\overline{B14}$	$\overline{B15}$	$\overline{P}$
	$\bar{A}\bar{J}$	$A\bar{B}$	$B\bar{C}$	$C\bar{D}$	$D\bar{E}$	$E\bar{F}$	$F\bar{G}$	$G\bar{H}$	$H\bar{I}$	$I\bar{J}$	AJ	$\bar{A}B$	$\bar{B}C$	$\bar{C}D$	$\bar{D}E$	$\bar{E}F$	$\bar{F}G$	$\bar{G}H$	$\bar{H}I$	$\bar{I}J$

4.3.3 Board S2 - Test Synthesis (Sequence Control) (3339512-1, 2)

Test programming selected by switches on the TCU front panel is implemented with the logic on board S2, Figure 4.3-4. When the start test switch has been actuated the next clock pulse (Px) will clock the Clock Control Flip Flop (FF1) initializing the sequency logic. Word frames will then be generated for each additional clock pulse word type decode gates then decode the frames into "A" word, "we" word, "D" words or "B" words which select the proper output multiplexer channels (SA and SB). Sequence control logic determines the types of words to be generated and the order of implementation.

For Write operations the number of blank words between each data word is controlled by the number of Blank Words Generator (BWG) and the Associated Control Logic. The desired number of blank words are set by No. B/W thumbwheel switches on the TCU front panel. The zero "B" words disables the BWG when no blank word spacing is desired. The reset logic provides the automatic resetting for each word cycle.

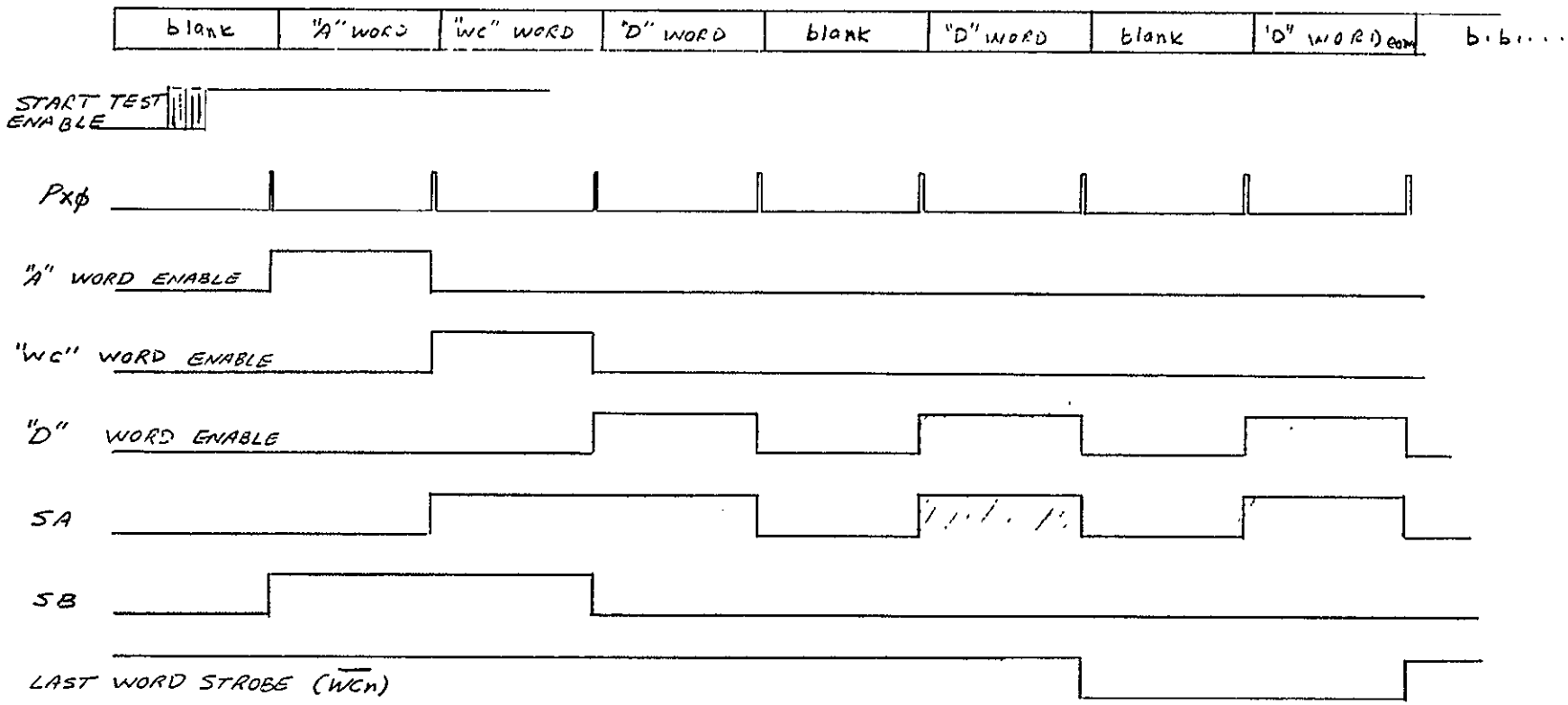
To determine the total length of each test sequence the count control section must keep track of the program progress. Inputs to the control logic determine when the count clock pulse is applied to the 16 bit word counter. Word count inputs from the word count switches on the front panel set the data field length. The word counter is implemented as a down counter and starts at the Word Count setting, and counts to zero. When the last word is detected by the last word decode logic, "D" word prefix bits are properly changed during write operations, and a last word strobe is generated to set up sequence termination logic. A strobe generated when the word count goes to zero sets up the Auto Reset Logic and provides the enable for the 8 bit Sequence Rate Counter. Once enabled the Sequence Rate Counter puts a number of blank words, determined by thumbwheel inputs, between each sequence frame. This spacing will allow for late data being returned from the DIU under test.



REF.
3339512-1 (SZ)
3339512-2

TEST SYNTHESIS (SEQUENCE CONTROL)

Figure 4.3-4



SIMPLIFIED TIMING FOR WRITE OPERATION WITH ONE BLANK WORD BETWEEN "D" WORDS

FIGURE 4.3-5

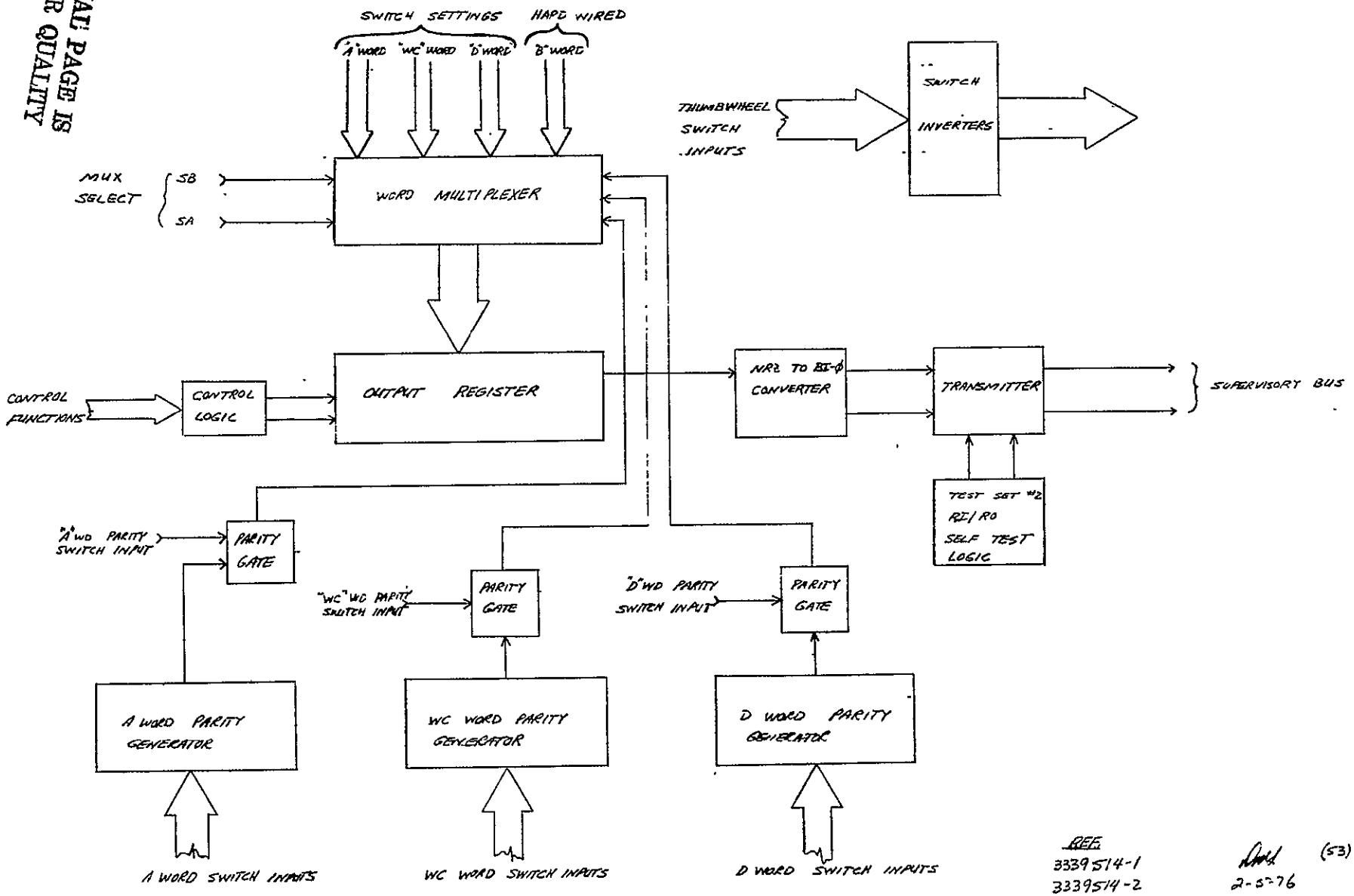
When the Sequence Rate count goes to zero the entire sequence control logic is reset. If the SINGLE/CONT. switch is set to CONT. the program repeats automatically. A simplified timing diagram depicting the basic timing functions is presented in Figure 4.3-5 for use as an aid in following the sequencer logic.

4.3.4 Board S3 - Supervisory Bus Interface (3339514-1, 2)

The block diagram of Figure 4.3-6 shows the data to be transmitted on the Supervisory Bus ("S" Bus), to the DIU under test. Data are entered into the Word Multiplexer via the word bits switches on the TCU front panel. Mux Select control lines explained in the previous section, 4.3.3, select the order in which the words are to be transmitted. The timing diagram of Figure 4.3-5 depicts a typical sequence.

From the multiplexer the Data are loaded broadside into the output shift register, on a command by the control logic. Once resident in the register the bits are shifted out serially to the NRZ to Bi-phase converter, then presented to the transmitter for transmission on the "S" Bus. The NRZ serial data are converted to Bi-phase by combining the data with the 2 MHZ system clock in an exclusive-OR gate. Encoding glitches are removed by clocking the resulting Bi-phase information through a flip-flop with the 4 MHz system clock, Figure 4.3-1. The transmitter circuitry employs a pair of push-pull transistors with Baker Clamp diodes to prevent saturation, and a center-tapped output transformer.

Parity Generators are utilized to program the parity bit attached to the end of each word transmitted, excluding the Blank Word. A provision for inserting parity errors has been incorporated by exclusive OR-ing the parity switch inputs with the outputs from the parity generators.



REF
3339514-1
3339514-2

(53)
2-5-76

SUPERVISORY BUS INTERFACE

Figure 4.3-6

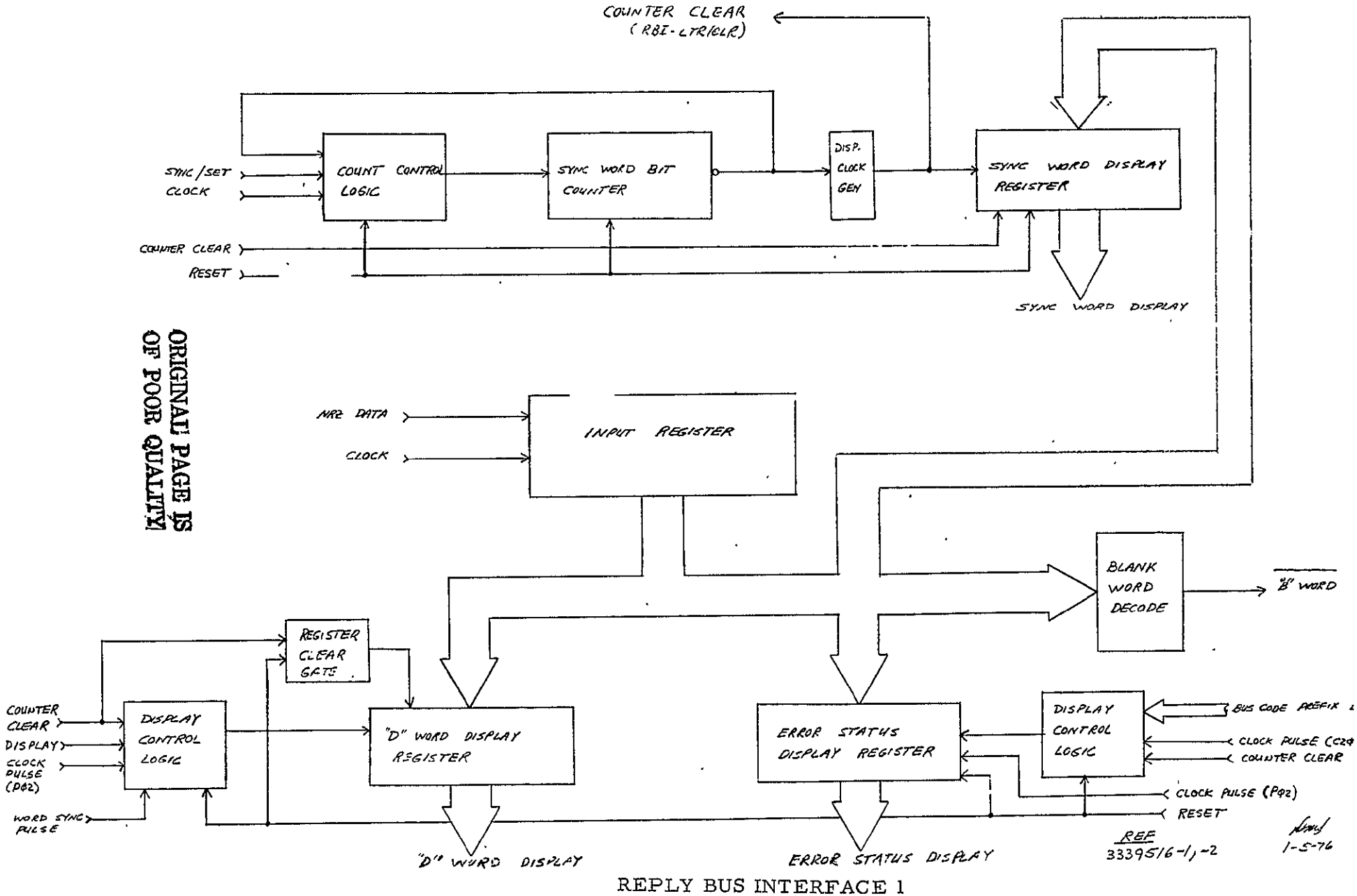
Inverters used to convert thumbwheel negative logic inputs into postive logic signals are included on this card. The remaining circuitry, self test logic, was employed to test the Sub System circuits of TCU number 2 during construction.

4.3.5 Board S4 - Reply Bus Interface 1 (3339516-1, 2)

The block diagram for Reply Bus Interface 1 is shown in Figure 4.3-7. Inputs from the Reply Bus are serially shifted into the Input Register then parallel loaded into the appropriate display registers. Since the sync word doesn't contain a full 20 bits of information it is treated separately. The first 12 bits shifted into the Input Register are loaded into the Sync Word Display Register, then a strobe is generated (CTR-CLK) to reset the Reply logic for normal 20 bit words. A Blank word decode ("$\overline{B}$" word) pulse is generated to reset the Reply timing Control logic during Blank word transmissions on the Reply Bus to ensure proper sync is maintained. Once resident in the display registers the outputs are displayed on the TCU front panel LED's. Buffer circuits are employed to reduce loading on the display registers output transistors these buffer/inverter boards are mounted in a separate fixture shown in Figure 4.2-1. The signals buffered by each card are labeled on this diagram.

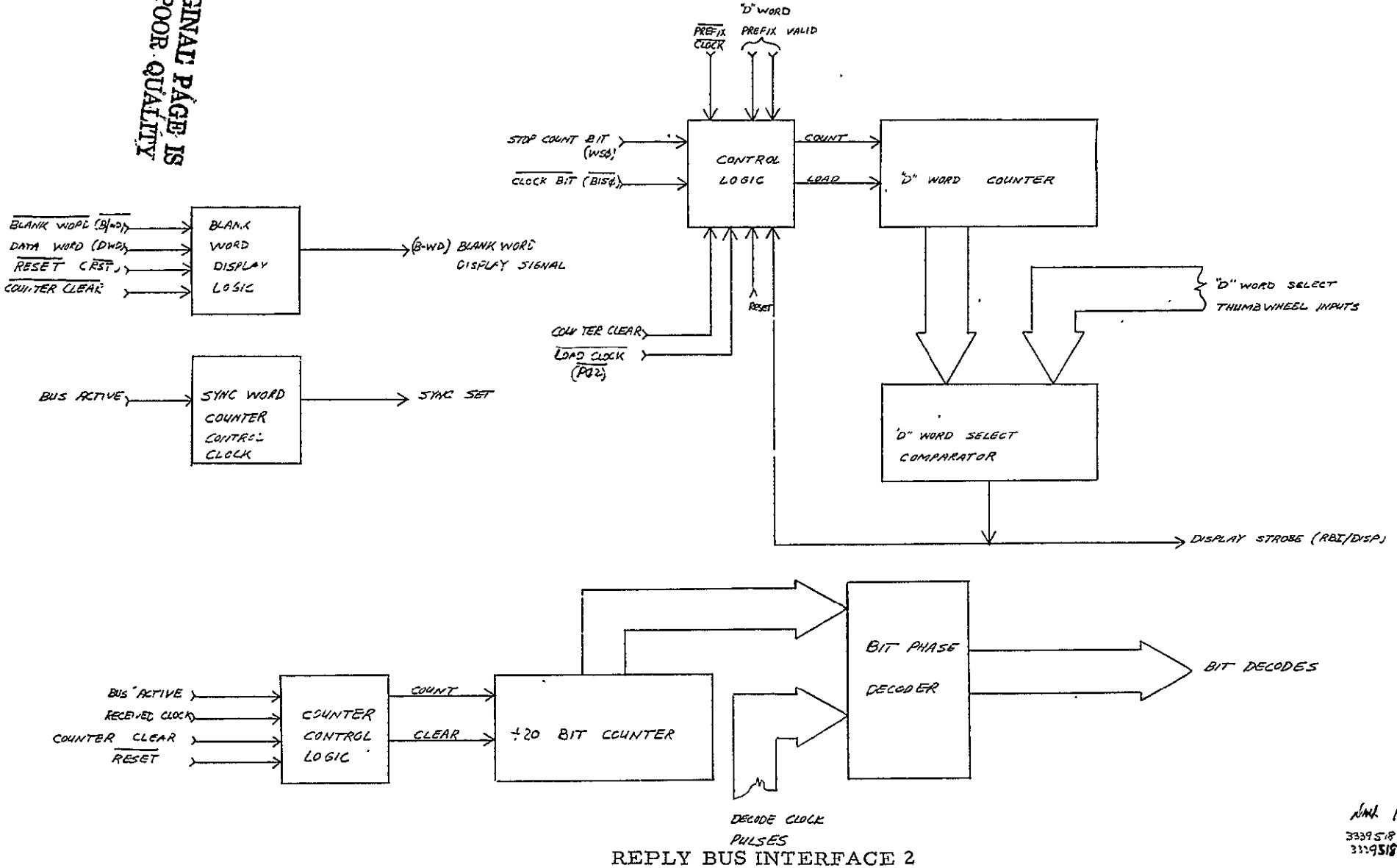
4.3.6 Board S5 - Reply Bus Interface 2 (3339518-1, 2)

Figure 4.3-8 depicts the block diagram for Reply Bus Interface 2. The basic timing for the Reply section of the TCU, exclusive of the timing for the Sync Word, is generated on this board. A 20 bit Johnson Counter identical to the one shown in Figures 4.3-1 and 4.3-3 is employed to generate the basic bit timing sequences. Counter control logic controls the count during the Sync Word time frame and reset it after the first 12 bits have been received. Instead of three bit phases running at a 4 MHz rate as was the case previously, the 2 MHz clock is combined with the outputs of the bit counter to obtain the bit decodes. This allows 2 bit phases per bit time.



REPLY BUS INTERFACE 1

Figure 4.3-7



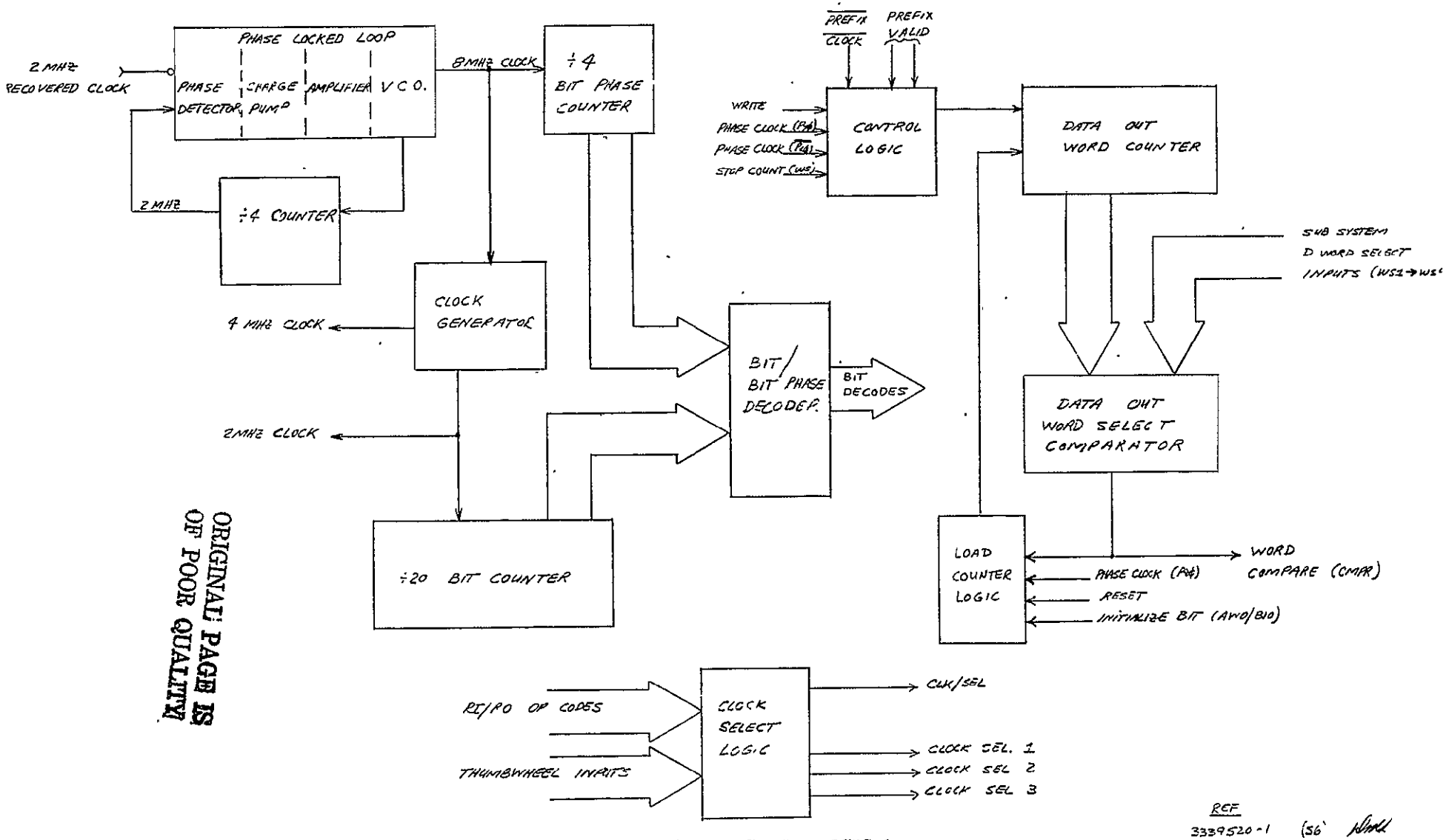
REPLY BUS INTERFACE 2
Figure 4.3-8

To be able to select "D" words on an individual basis a "D" word counter and "D" word select comparator are employed. The "D" word Counter looks for data words in the received information and counts each one received. This count is broadside loaded into a comparator and weighed against data presented via "D" word select thumbwheel switches. When the count matches the thumbwheel setting a Display Strobe (RBI-DISP) is generated to load the display register. To ensure only "D" words are counted the control logic examines the prefix bits of each word allowing only "D" words to be counted. Once the desired word has been found the control logic resets the "D" word Counter to zero.

Additionally, the sync word enable clock pulse (sync set) is activated by the Bus Active Signal generated by the receiver circuitry. Undesirable transmitter turn on characteristics are avoided by disabling the 2 MHz clock to the Sync Word count Control logic, Figure 4.3-7, until transients have subsided. An additional circuit provides for the detection and display of the first blank word received on the Reply Bus after the Sync word. If the word following the Sync word is a Blank word the "B" word display LED (single LED) is illuminated on the TCU front panel. If a data word precedes the first Blank word the LED stays off. In any event the Blank word Display Logic is reset at the end of each DIU transmission.

4.3.7 Board S6 - Sub System Synthesis 1 (3339520-1, 2)

Sub System Synthesis 1 block diagram is shown in Figure 4.3-9. Clock synchronization is implemented with the phase-locked loop circuitry. The 2 MHz recovered clock and the loop generated 2 MHz clock are supplied to a phase comparator. This circuit generates an error signal proportional to the phase difference between the two clocks. The charge pump in concert with the amplifier inverts one of input wave forms from the phase detector and translates the voltage levels before they are applied to the loop filter.



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REF
3339520-1 (56)
3339520-2

8-6-76

SUB SYSTEM SYNTHESIS 1

Figure 4.3-9

Therefore, the output of the amplifier will "pump up" to raise the VCO frequency and "pump down" to lower the frequency. The low-pass filter controls the fundamental loop characteristics such as signal capture range, loop bandwidth, capture time, and transient response. The VCO frequency is set to lock at 8 MHz which is then used as the System 8 MHz clock. A ÷ 4 counter in the feedback loop reduces the 8 MHz to the internal 2 MHz clock, which is compared to the recovered clock.

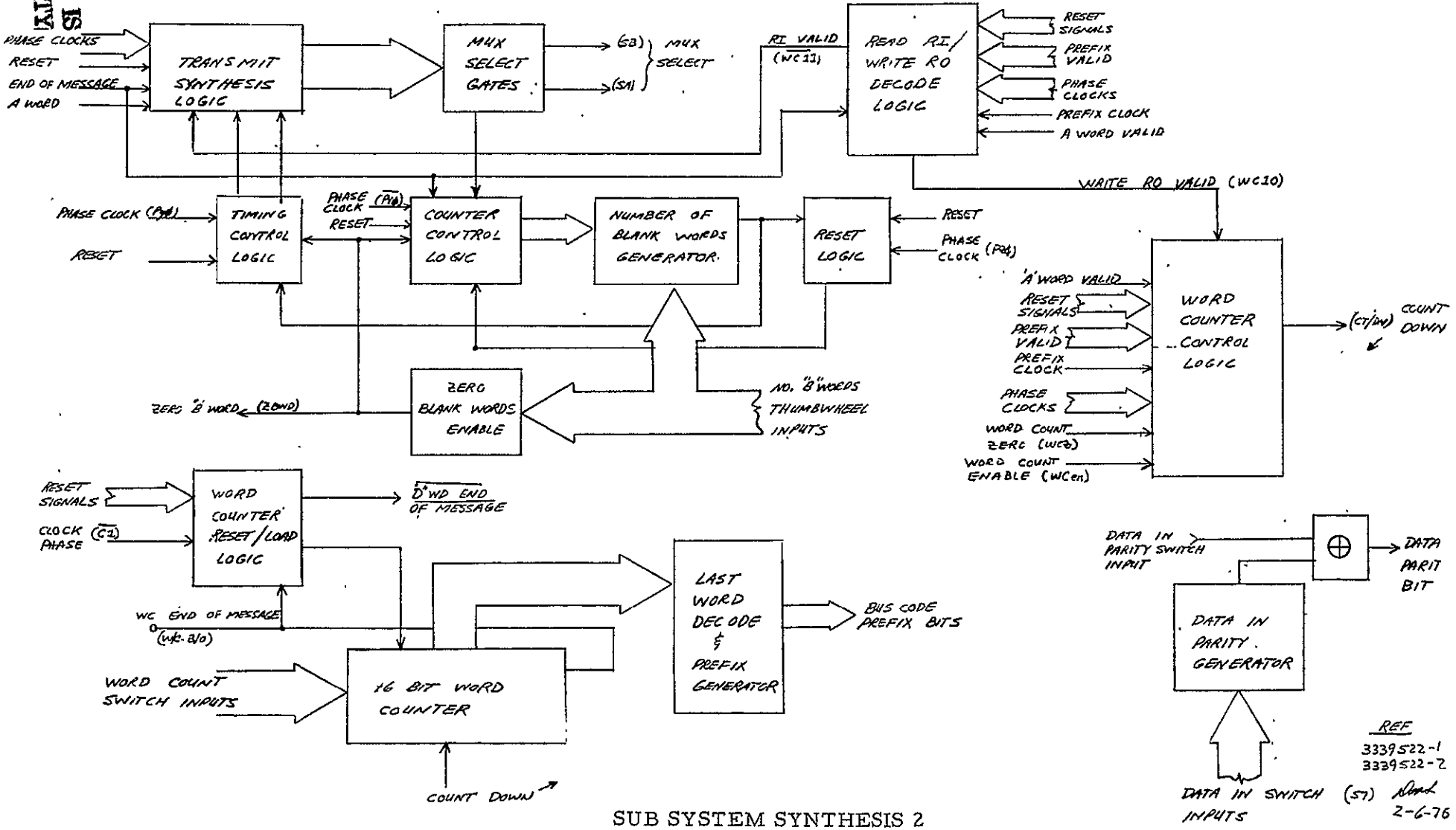
A ÷ 4 bit phase counter and a ÷ 20 bit counter, essentially the same as those shown in Figure 4.3-1, 4.3-2, and 4.3-3, provide the timing signals for the Sub System timing decode signals. The 20 bit counter is reset to a different state (all zero's) than is shown in Figure 4.3-3, but the decodes will only be shifted by one bit time. The clock generator is a binary counter that reduces the 8 MHz to the needed 4 MHz and 2 MHz system clocks.

The Data Out word counter, Data Out word select comparator, and the associated control, reset, logic is the same as that described in Section 4.3.6 and shown in Figure 4.3-8. The difference being that the data is being presented to a sub system from the DIU under test instead of being supplied to the CIU interface (Reply bus).

Circuitry to invert the RO clock select thumbwheel inputs and to define the proper op code is provided. The thumbwheel inputs are converted to true logic and the op codes are later combined to give a clock/select enable signal.

4.3.8 Board S7 - Sub System Synthesis 2 (3339522-1, 2)

Figure 4.3-10 shows the block diagram of Sub System Synthesis 2 logic board. The logic contained on this card performs essentially the same function as board S2, Section 4.3.3. Transmit synthesis logic provides the correct word



SUB SYSTEM SYNTHESIS 2

Figure 4.3-10

sequences to be transmitted. These word frames (BWD, DWD and E/S) are supplied to the mux select gates which in turn controls the output multiplexer channel selection. As was done in Section 4.3.3 a blank word generator enables a variable number of blank words to be inserted between each Data In word. The zero "B" word (E BWD) signal generated on this card is fed back to card S2, and its purpose is explained in that section.

The word counter, reset/load logic, and decode circuits are essentially the same as those explained in Section 4.3.3 and shown in Figure 4.3-4. To initiate sub system activity the correct RI/RO prefix bits are decoded from the word count word along with the correct op code contained in the "A" word. Data In parity bit is generated in the same manner as described for the command words. Error Status parity is set manually.

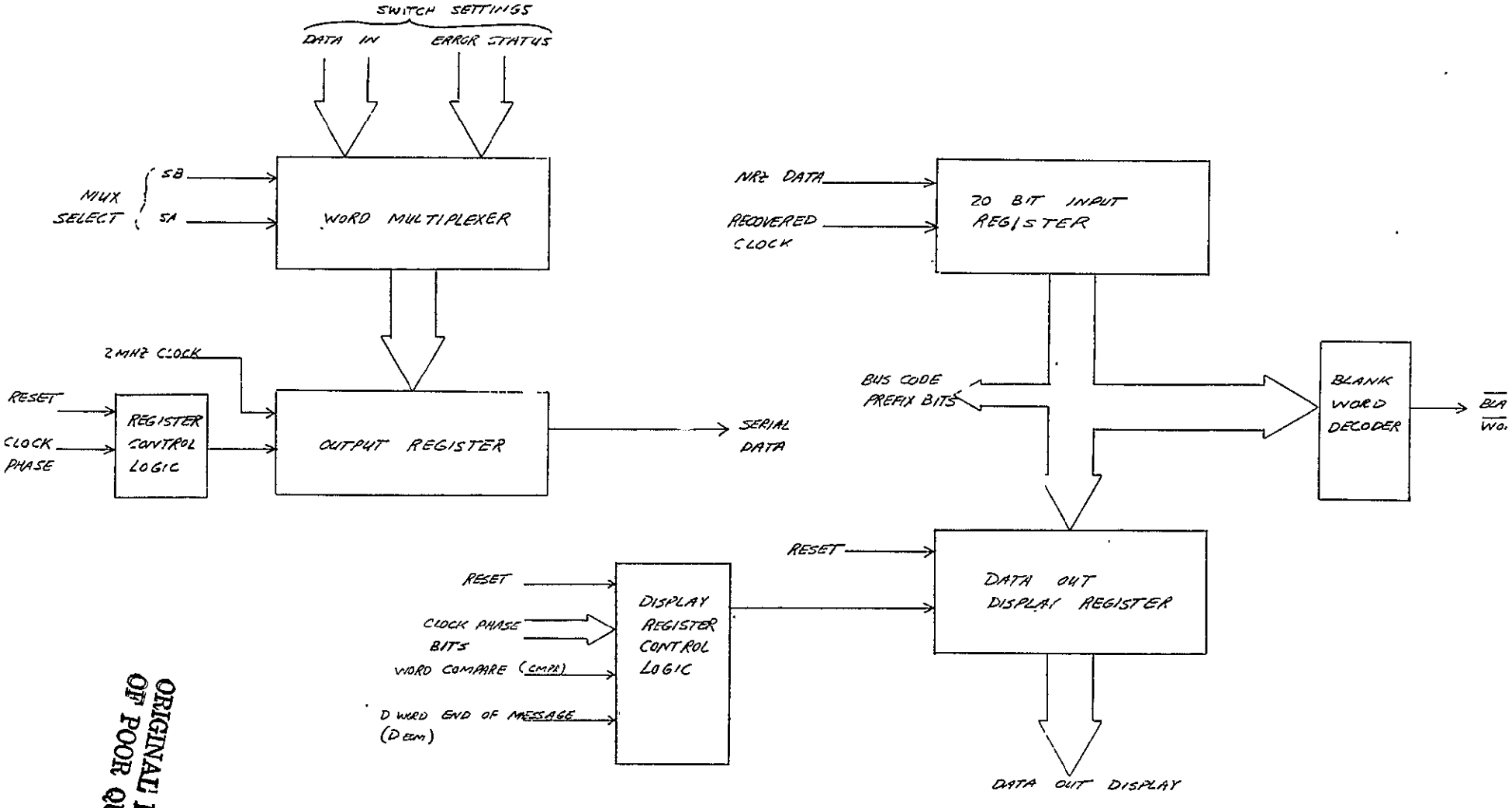
4.3.9 Board S8 - Sub System Synthesis 3 (3339524-1, 2)

The block diagram shown in Figure 4.3-11 shows the logic circuitry contained on board S8-Sub System Synthesis 3. The serial output data/word multiplexer logic is the same as that discussed in Section 4.3.4 and shown in Figure 4.3-6.

The 20 bit input register accepts the data from the RI/RO bus receiver then outputs this data in parallel for bus code prefix identification, blank word sync strobe ($\overline{\text{Blank Word}}$) generation, and Data Out Display. The Blank Word Decoder and the Data Out Display circuits have been described in Section 4.3.5 and shown in Figure 4.3-7. The timing pulses and resets are different due to the nature of the Sub System Interface requirements.

4.3.10 Board S9a - RO Clock Receiver (3339526-1)

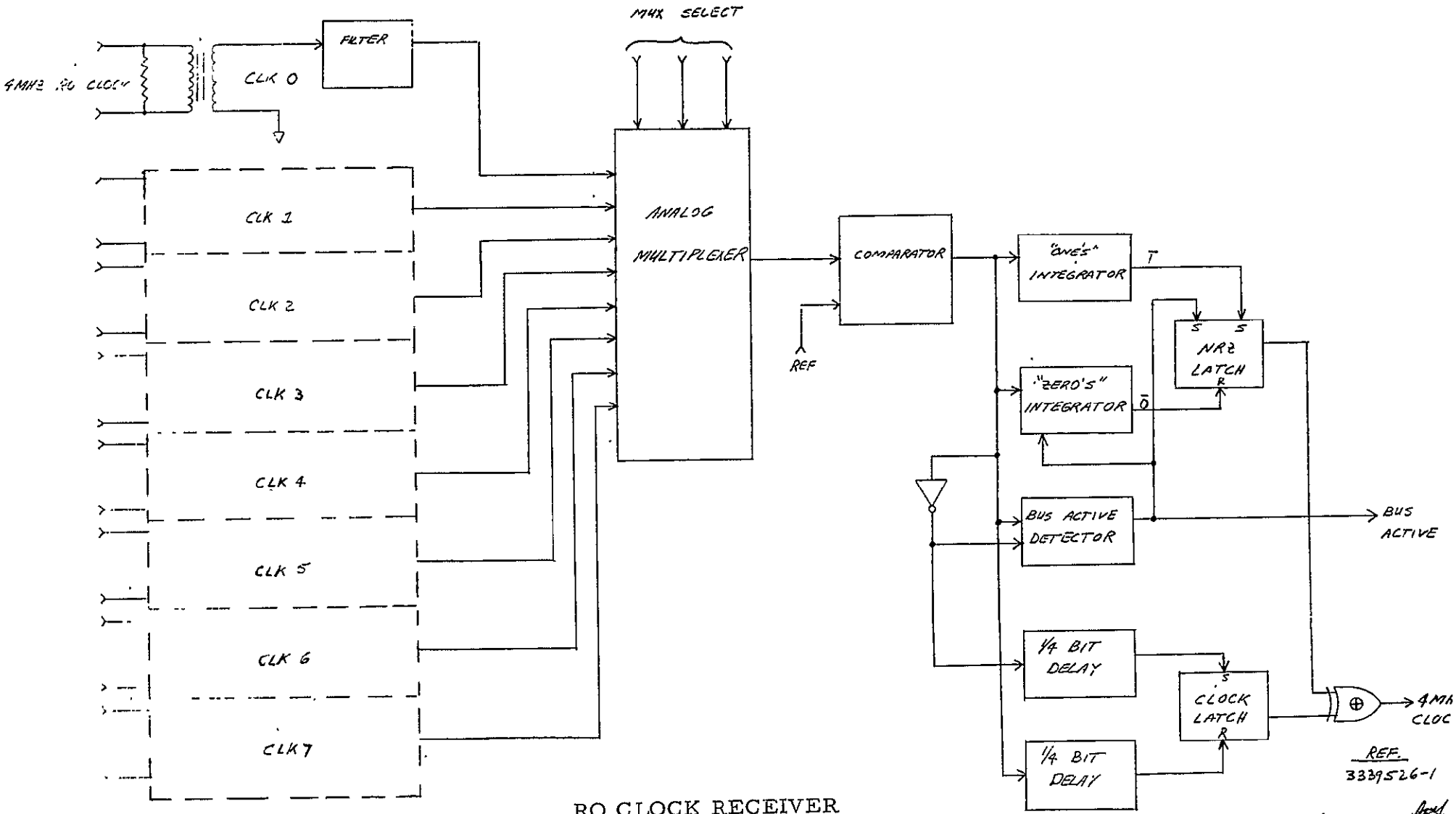
The RO clock Receiver block diagram is shown in Figure 4.3-12. From the comparator section through the receiver outputs the circuitry is the same



SUB SYSTEM SYNTHESIS 3

Figure 4.3-11

REF
3339524-1 (SB)
3339524-2 2-6-76



RO CLOCK RECEIVER

Figure 4.3-12

as the bus receivers. Section 4.3.11 describes the bus receiver operation which is shown in Figure 4.3-13. The 8 RO clock lines are connected to an input filter which is the same configuration as that used for all of the bus receivers, but it's cutoff frequency has been raised to accept the 4 MHz clock. The only significant addition to the receiver is the addition of an input multiplexer. The mux select signals are derived from clock select thumbwheel inputs, to select the appropriate channel as defined in the "A" word.

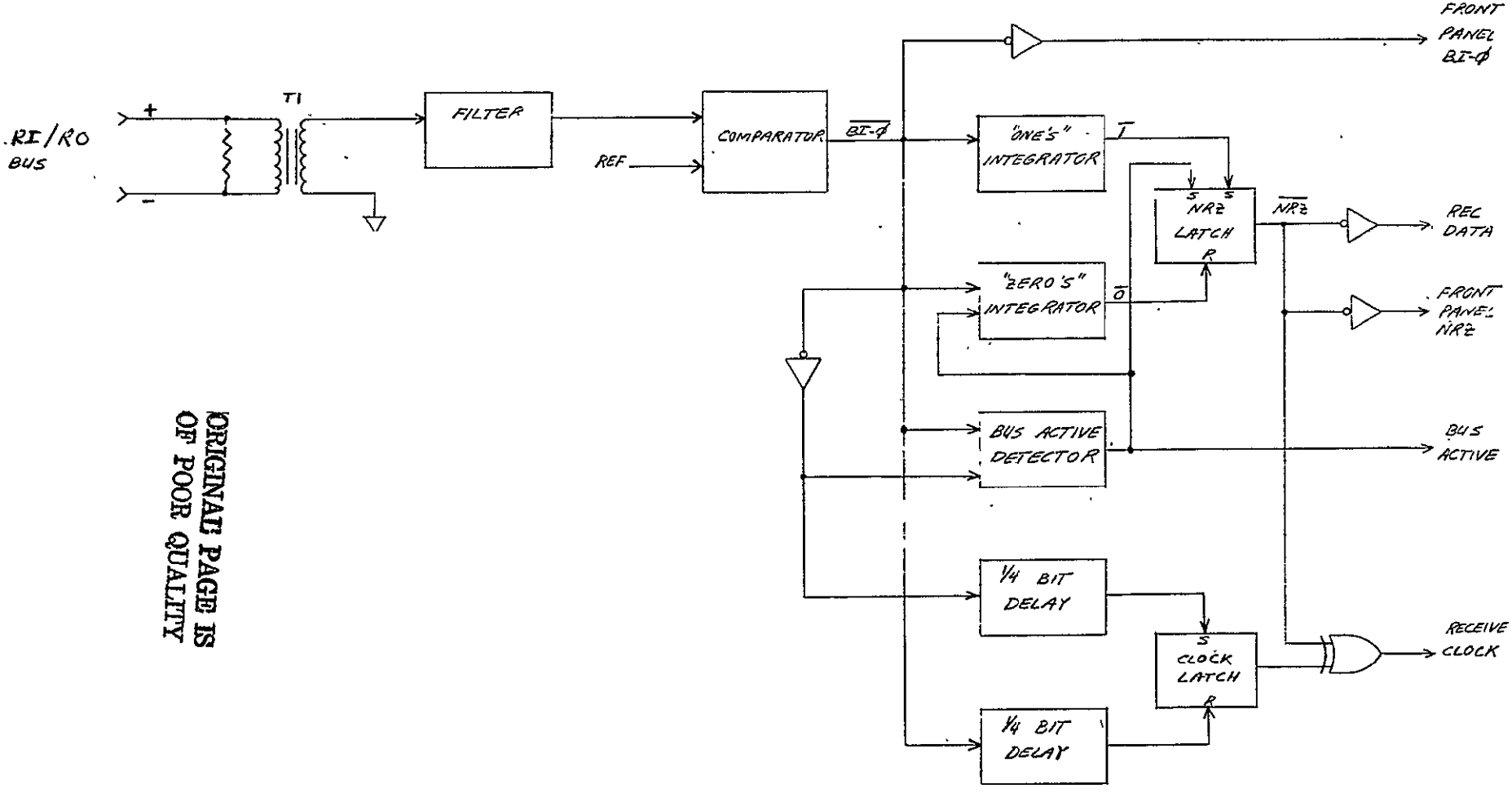
4.3.11 RI/RO Bus Receiver (3339526-2)

The bus receiver accepts continuous bi-phase data from the DIU Interface bus and performs bi-phase to NRZ conversion using pulse integration techniques. The block diagram is shown in Figure 4.3-13.

The front end of the receiver consists of an isolation transformer and a raised-cosine input filter. The filter provides 6 db attenuation at twice the bit rate, and is optimized for minimum intersymbol interference for bi-phase data.

The filter output is supplied to a voltage comparator, which is biased at approximately 250 mv. Voltage feedback is included to provide approximately 5 mv. of hysteresis at the comparator reference input. The hysteresis prevents oscillation at the comparator output due to slow rise times at the filter output.

The comparator output is buffered for a front panel test point, and also supplied to two integrators, a bus-active detector, and the clock generator delay circuits.



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3339526-2

RI/RO BUS RECEIVER

Figure 4.3-13

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The outputs of the "One's" integrator and "Zero's" integrator supply set and reset signals to the NRZ latch. The Bus Active detector sets the NRZ latch to a "One's" condition and discharges the "Zero's" integrator when the RI/RO bus is inactive.

The comparator output is also supplied to two 1/4 bit delay circuits to synchronize the clock and data outputs. The outputs of the Clock latch and the NRZ latch are Exclusive OR'ed to generate the Receive clock. The NRZ latch is buffered for a front panel test point and the Receive Data signal.

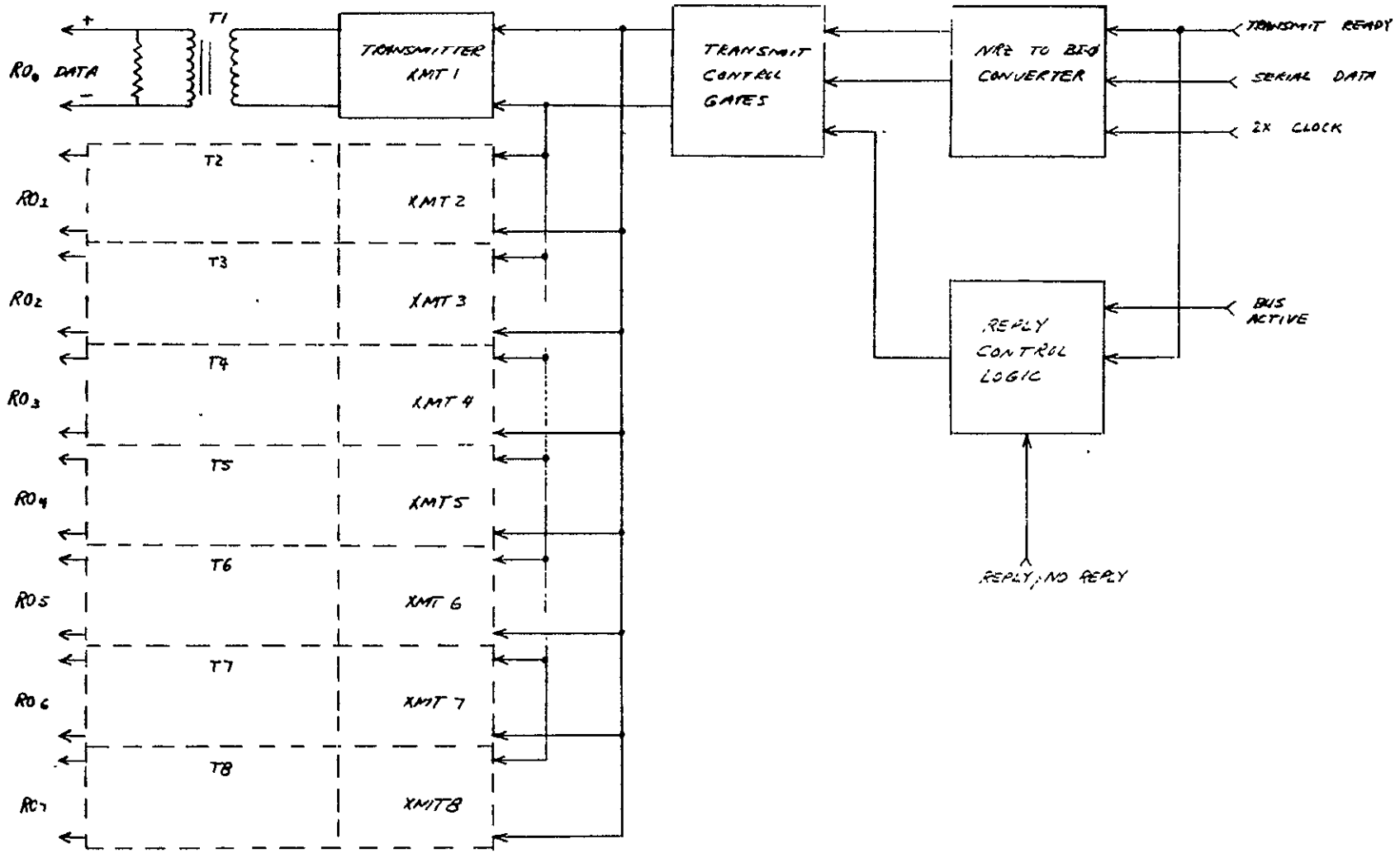
4.3.12 Board S10 - RI Transmit Logic (3339528)

Figure 4.3-14 shows the RI transmit logic block diagram. The 8 transmitters and the NRZ to BI-phase converter are identical to those described in Section 4.3.4 and shown in Figure 4.3-6. The transmit control logic and control gates are used to start and stop the transmitter at the correct times. Included in the control logic is a provision for inhibiting the transmitters when no sub system reply is desired. To avoid premature transmitter turn-on an enable delay flip-flop has also been incorporated using the BUS ACTIVE signal as its data input.

4.3.13 Board S11 - Signal Conversion (3339530-1, 2)

The block diagram of the Signal Conversion board is shown in Figure 4.3-15. The "B" side of this board contains the Reply Bus Receiver whose operation is explained in Section 4.3.11 and shown in Figure 4.3-13. The "D" word inverters interface the thumbwheel inputs to the Data Out comparator inputs, Figure 4.3-9.

The sub system clock decoder is a 3 line to 8 line decoder used to select the RO clock displayed on the TCU front panel. The clock select enable is derived from the "A" word op codes for RI/RO instructions.



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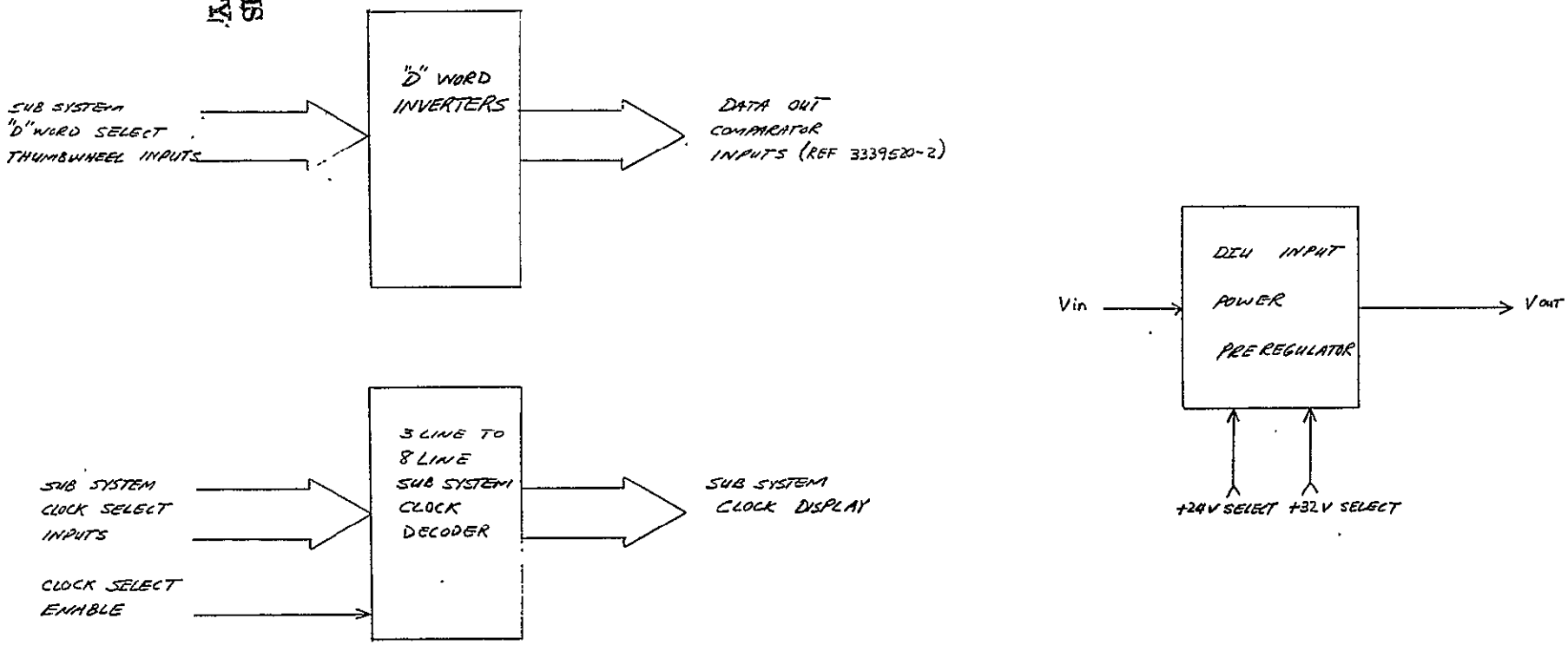
RI TRANSMIT LOGIC

Figure 4.3-14



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3339530-1

SIGNAL CONVERSION

Figure 4.3-15

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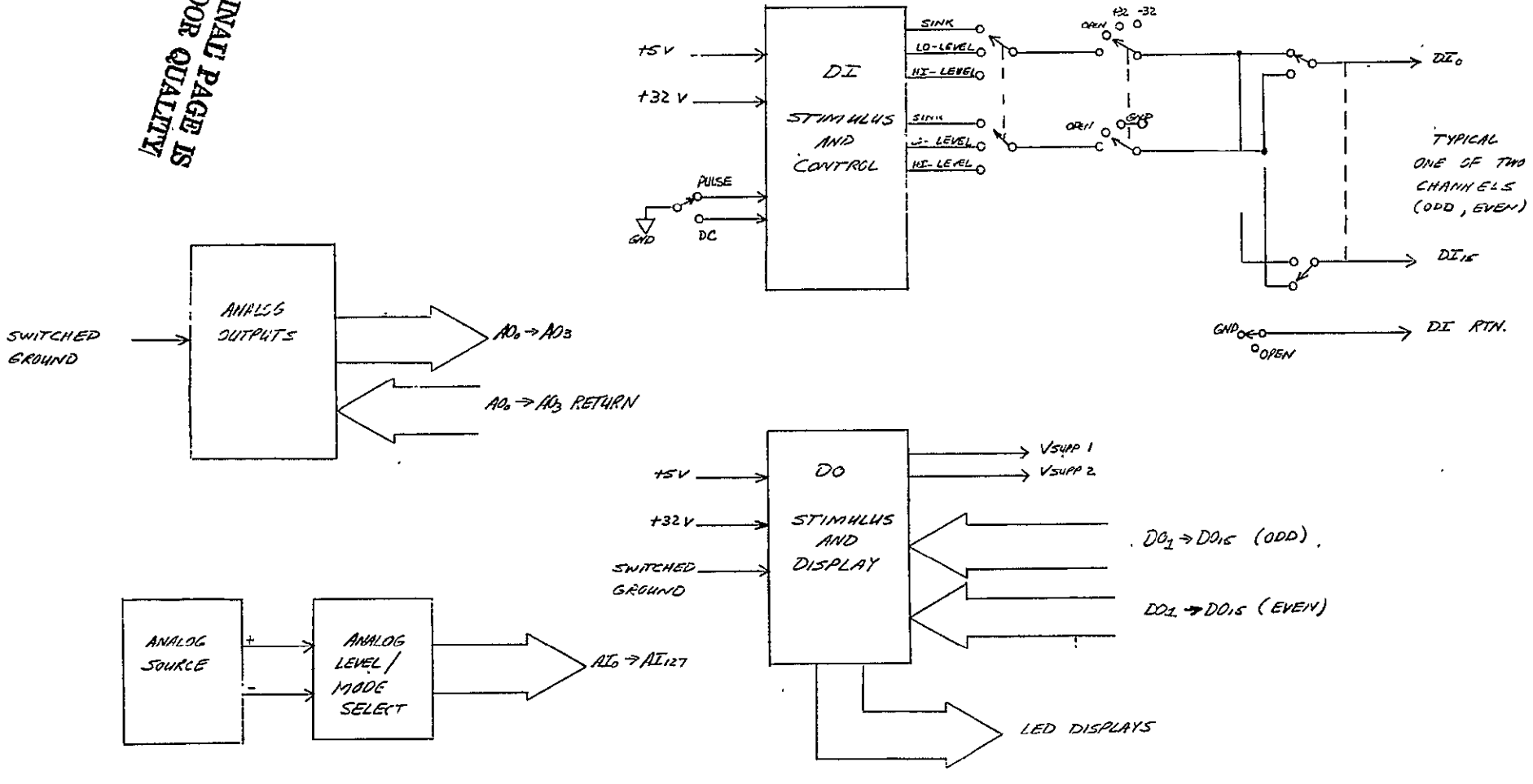
a

A DIU power preregulator circuit has been incorporated to allow over voltage and under voltage source testing of the DIU under test. The TCU front panel power select switch is used to select the desired voltage level while the preregulator minimizes the transients presented to the DIU during switch setting changes.

4.3.14 DIU Stimulus Panel (3339550, 3339580)

The block diagram of the DIU Stimulus Panel is shown in Figure 4.3-16. Section 3 of this report details the operation of the Stimulus Panel and should be consulted if any troubleshooting is necessary. The drawings in Appendix A, the discussion in Section 3, and this block diagram should allow for effective troubleshooting.

A simplified drawing of typical switch selectable programming is shown for the DI Stimulus and Control group. The switches show the various program postions called out in Section 3.3.



STIMULUS PANEL

Figure 4.3-16

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3339580

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